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PCIe to Fiber Converter

Interface Control Document

PFC ICD

Document History

Revision	Date	Author	Details
1.0	14-Jul-2022	IA	Initial release
1.1	20-Jul-2022	IA	1. Section 10. Updated LED table 2. Section 12. Updated thermal performance
1.2	28-Jul-2022	IA	1. Section 6. Updated front panel drawing 2. Section 10. Updated LED table
1.3	8-Sep-2022	IA	1. Section 7.4. Updated axillary signal description 2. Section 9.2. Updated S1 DIP switch description

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1 Scope

This document controls all interfaces between the PCIe to Fiber Converter (PFC) and the external environment.

2 Applicable and Reference Documents

2.1 Applicable Documents

AD-1: PCI Express External Cabling Specification, Revision 2.0
AD-2: PCI Express Base Specification, Revision 2.1
AD-3: SFF-8436 QSFP+ 4X 10 Gb/s Pluggable Transceiver, Revision 4.9

3 Terms and Acronyms

Table 3-1 Terms and Acronyms

Term	Description
x8	A Link with eight Physical Lanes.
AOC	Active Optical Cable
Downstream Subsystem	The relative position of an interconnect component that is farther from the Root Complex.
Gb/s	Gigabit per second
Gen 2	PCIe 5 Gb/s speed
Lane	A set of differential signal pairs, one pair for transmission and one pair for reception. A by-N Link is composed of N *Lanes*
Link	The collection of two Ports and their interconnecting Lanes.
NC	Not connected
QSFP	Quad Small Form-Factor Pluggable Transceiver
PCIe	Interconnect standard for PCI Express cards
PFC	PCIe to Fiber Converter
Root Complex	A device that connects the processor and memory subsystem to the PCI Express switches and devices
SSC	Spread Spectrum Clock
Upstream Subsystem	The relative position of an interconnect component that is closer to the Root Complex.

4 Introduction

The PFC is designed to extend a standard PCIe x8 cable defined in the PCI Express External Cabling Specification (AD-1) over two QSFP Active Optical Cables (AOC). The PFC converts a PCIe x8 cable upstream and downstream interfaces into two QSFP interfaces compatible with standard AOCs. A PCIe x8 over fiber optic extension system consists of a host and target PFCs connected by two 40Gb/s QSFP active optical cables (AOC). The host PFC is connected to a PCIe cable interface card in the computer via an iPass PCIe x8 cable. The PCIe endpoint is connected to the target PFC via the second iPass PCIe x8 cable. The system block diagram is shown in Figure 4-1.

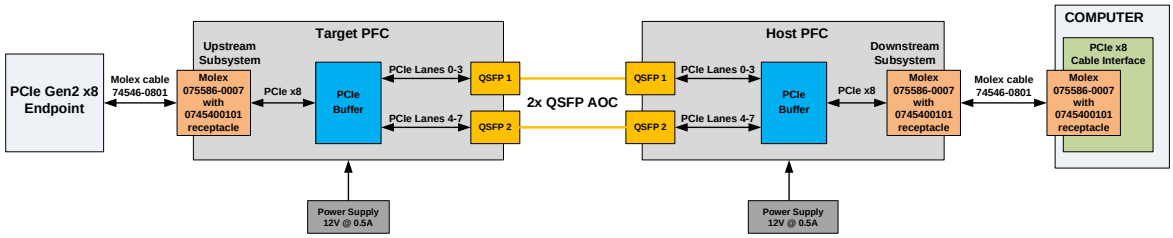

Figure 4-1 System Block Diagram

The host and target PFCs are the same but operate in different modes. The PCIe interface in the host PFC is configured as a downstream subsystem. The PCIe interface in the target PFC is configured as an upstream subsystem. The extension is transparent to the PCIe link protocol and does not contain PCIe switches and retimers. The PFC uses PCIe buffers to interface QSFPs to standard PCIe upstream and downstream ports. The buffers feature a continuous time linear equalizer that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects. The equalization is programmable by DIP switches to compensate for losses in the iPass cables.

The PFC supports all standard axillary signals. The PFC extension uses the Separate Refclk with no SSC (SRNS) architecture. The PCIe clock is not transferred from the host to the target over the AOCs. The target PFC generates a separate constant 100 MHz PCIe clock. The PCIe cable interface card in the computer must provide spread spectrum clock isolation and use a 100 MHz constant clock for the PCIe cable port.

5 Interface-Context Diagram

The following Interface Context Diagram in Figure 5-1 below is intended to provide a convenient reference and "road map" to this document. Each interface is shown on the Context Diagram, with a type descriptor (PCIe, QSFP, Mechanical, etc.).

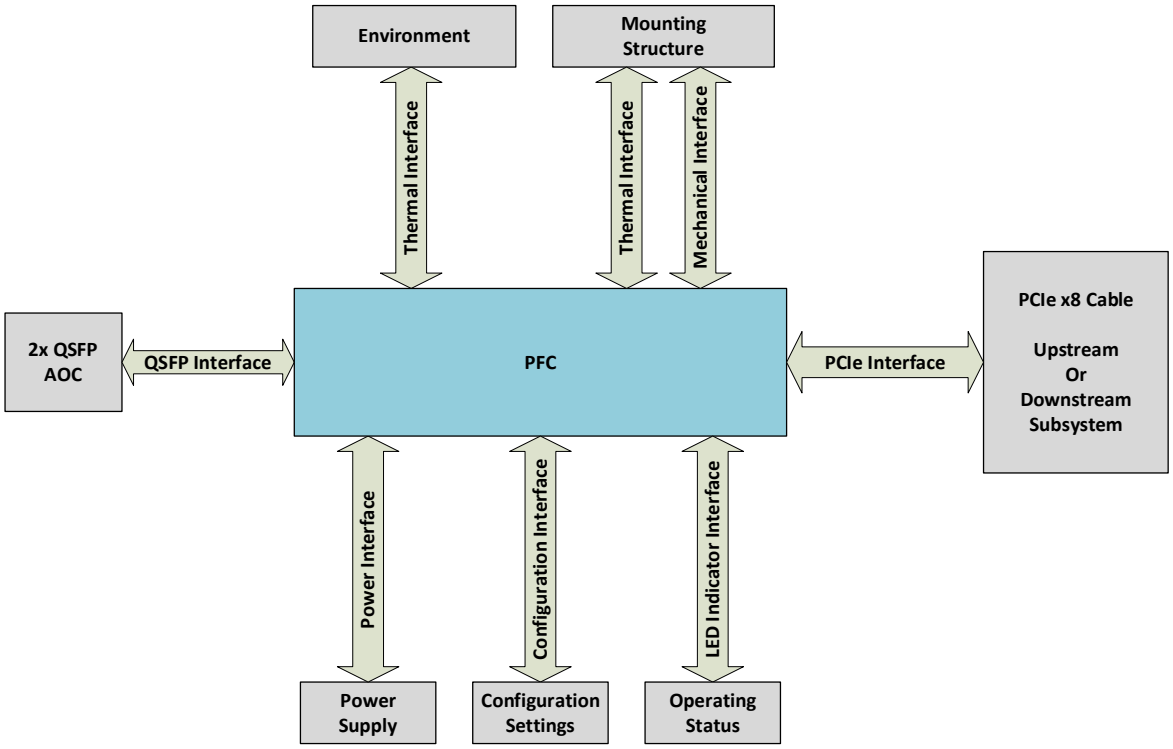

Figure 5-1 Interface-Context Diagram

6 Mechanical Interface

6.1 Description

The PFC electronics are mounted in a customized extruded aluminum enclosure equipped with a flanged frame for easy wall mounting. The PFC dimensions are shown in Figure 6-1.

Part number: EXPF11-4-13
Manufacturer: TAKACHI ELECTRONICS ENCLOSURE CO., LTD.
Detailed drawings: https://www.takachi-enclosure.com/products/EXPF
Mechanical model: PFC_10_2022-07-28.stp

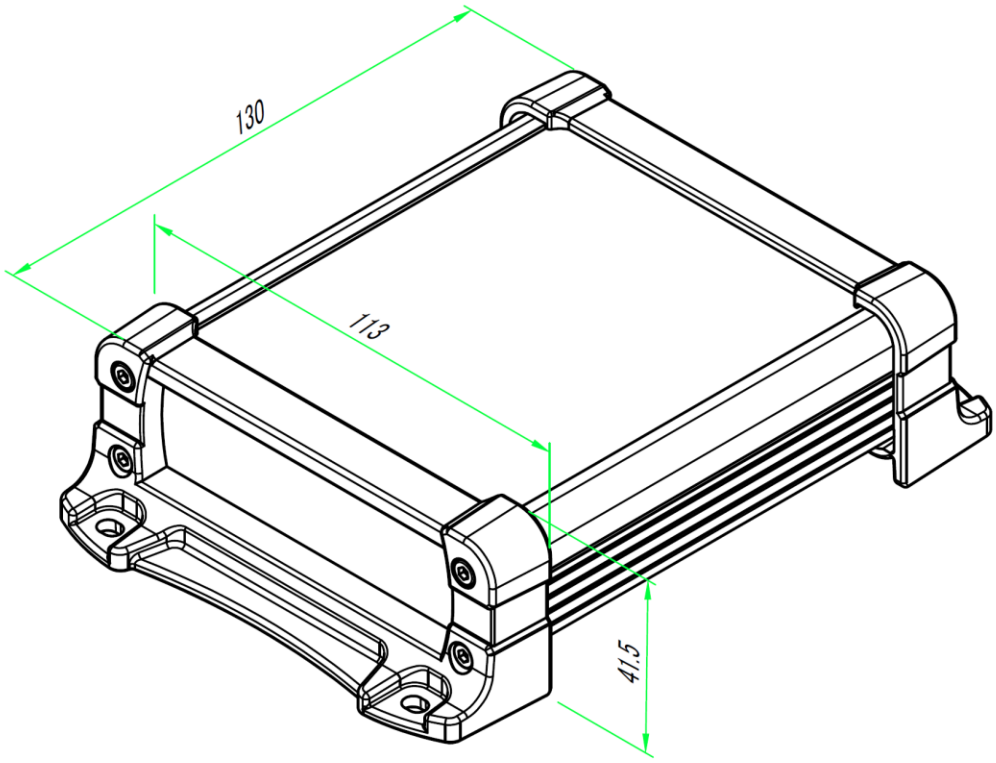

Figure 6-1. PFC Dimensions in mm.

All external connectors are mounted on the front and back panels. The panel drawings are shown in Figure 6-2 and Figure 6-3.

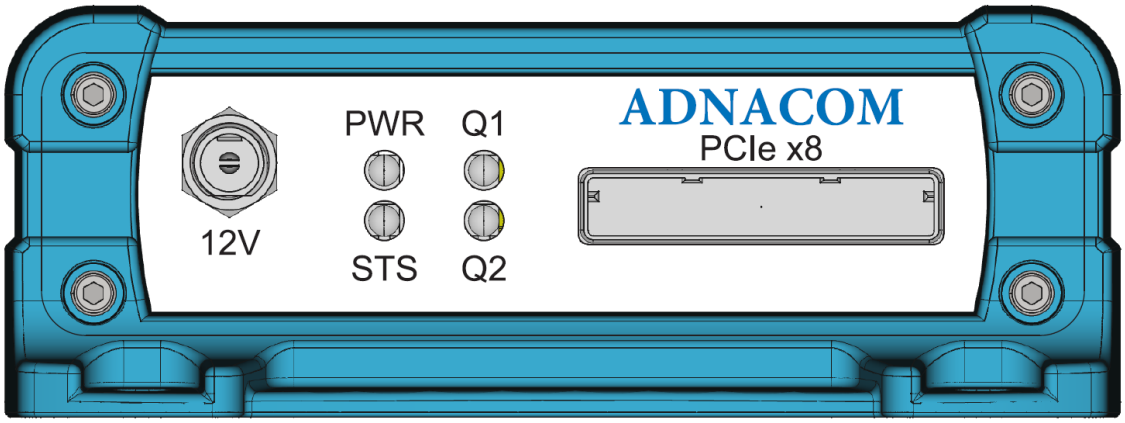

Figure 6-2. PFC Front Panel

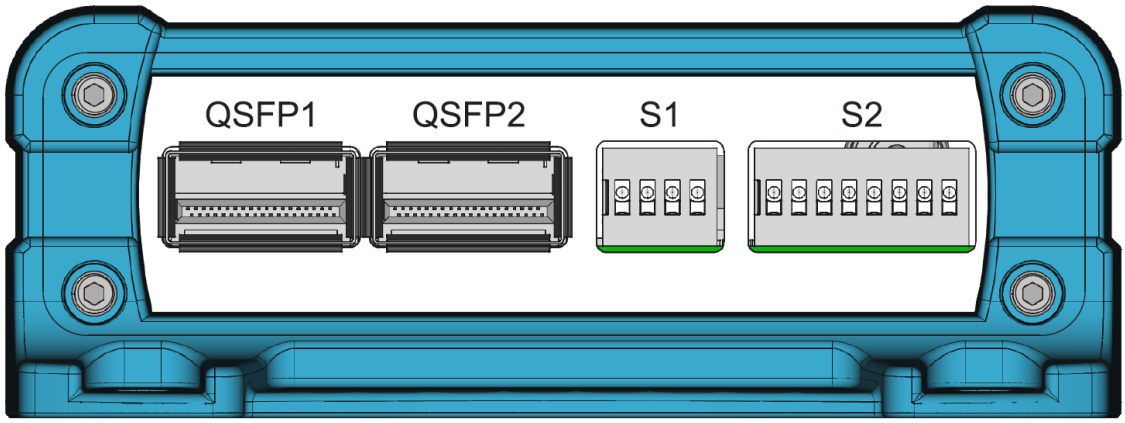

Figure 6-3. PFC Back Panel

The PCIe x8 connector is described in section 7.
The LED indicators are described in section 10.
The 12V power connector is described in section 11.
The QSFP1 and QSFP2 connectors are described in section 8.
The S1 and S2 DIP switches are described in section 9.

7 PCIe Interface

7.1 Description

The PCIe interface is compliant with the following specifications:

- PCI Express External Cabling Specification (AD-1)
- PCI Express Base Specification (AD-2)

The PCI interface supports:

- PCIe x8 external cable
- PCIe Gen 2 (5 Gb/s) speed
- Operation in upstream or downstream mode
- Standard auxiliary signals
- 100 MHz constant reference clock

7.2 Connector Type

Type: iPass I/O Surface Mount Receptacle, 68 Pins
Part number: 0755860007
Manufacturer: Molex

Type: PCIe Guide Frame, x8
Part number: 745400101
Manufacturer: Molex

7.3 Connector Pin Assignments

This information supersedes the information in the RD-1.

Table 7-1 P3 Pin Assignments

Pin	PCIe x8	Description	Downstream	Upstream
A1	GND	Ground	GND	GND
A2	PETp0	PCIe TX Lane 0	PETp0	PETp0
A3	PETn0		PETn0	PETn0
A4	GND	Ground	GND	GND
A5	PETp1	PCIe TX Lane 1	PETp1	PETp1
A6	PETn1		PETn1	PETn1
A7	GND	Ground	GND	GND
A8	PETp2	PCIe TX Lane 2	PETp2	PETp2
A9	PETn2		PETn2	PETn2
A10	GND	Ground	GND	GND
A11	PETp3	PCIe TX Lane 3	PETp3	PETp3
A12	PETn3		PETn3	PETn3
A13	GND	Ground	GND	GND
A14	CREFCLKp	Reference Clock	See Table 7-2	See Table 7-3
A15	CREFCLKn			

A16	GND	Ground	GND	GND
A17	RSVD	Reserved	NC	NC
A18	RSVD	Reserved	NC	NC
A19	SB_RTN	Sideband Signals Return	GND	GND
A20	CPRSNT#	Cable Present	See Table 7-2	See Table 7-3
A21	CPWRON	Cable Power On	See Table 7-2	See Table 7-3
A22	GND	Ground	GND	GND
A23	PETp4	PCIe TX Lane 4	PETp4	PETp4
A24	PETn4		PETn4	PETn4
A25	GND	Ground	GND	GND
A26	PETp5	PCIe TX Lane 5	PETp5	PETp5
A27	PETn5		PETn5	PETn5
A28	GND	Ground	GND	GND
A29	PETp6	PCIe TX Lane 6	PETp6	PETp6
A30	PETn6		PETn6	PETn6
A31	GND	Ground	GND	GND
A32	PETp7	PCIe TX Lane 7	PETp7	PETp7
A33	PETn7		PETn7	PETn7
A34	GND	Ground	GND	GND
B1	GND	Ground	GND	GND
B2	PERp0	PCIe RX Lane 0	PERp0	PERp0
B3	PERn0		PERn0	PERn0
B4	GND	Ground	GND	GND
B5	PERp1	PCIe RX Lane 1	PERp1	PERp1
B6	PERn1		PERn1	PERn1
B7	GND	Ground	GND	GND
B8	PERp2	PCIe RX Lane 2	PERp2	PERp2
B9	PERn2		PERn2	PERn2
B10	GND	Ground	GND	GND
B11	PERp3	PCIe RX Lane 3	PERp3	PERp3
B12	PERn3		PERn3	PERn3
B13	GND	Ground	GND	GND
B14	PWR	+3.3 V Power	See Table 7-4	See Table 7-4
B15	PWR	+3.3 V Power		
B16	PWR	+3.3 V Power		
B17	PWR_RTN	Ground	GND	GND
B18	PWR_RTN	Ground	GND	GND
B19	PWR_RTN	Ground	GND	GND
B20	CWAKE#	Cable WAKE	See Table 7-2	See Table 7-3
B21	CPERST#	Cable Platform Reset	See Table 7-2	See Table 7-3
B22	GND	Ground	GND	GND
B23	PERp4	PCIe RX Lane 4	PERp4	PERp4
B24	PERn4		PERn4	PERn4
B25	GND	Ground	GND	GND
B26	PERp5	PCIe RX Lane 5	PERp5	PERp5
B27	PERn5		PERn5	PERn5
B28	GND	Ground	GND	GND

B29	PERp6	PCIe RX Lane 6	PERp6	PERp6
B30	PERn6		PERn6	PERn6
B31	GND	Ground	GND	GND
B32	PERp7	PCIe RX Lane 7	PERp7	PERp7
B33	PERn7		PERn7	PERn7
B34	GND	Ground	GND	GND

7.4 Auxiliary Signals

Table 7-2. Downstream System Side-Band Signals (Host).

Signal	Signal Type	
CREFCLK	Termination	Dual 50 Ω termination to ground.
CPRSNT#	3.3 V Logic	Open-drain output. High impedance during the power-off state. Always low in the power-on state.
CPERST#	3.3 V Logic	Input with pull-down resistor from 25 to 55 kΩ. High impedance during the power-off state.
CPWRON	3.3 V Logic	Input with pull-down resistor from 25 to 55 kΩ. High impedance during the power-off state.
CWAKE#	3.3 V Logic	Open-drain output. High impedance during the power-off state. Always high in the power-on state.

Table 7-3. Upstream System Side-Band Signals (Target).

Signal	Signal Type	
CREFCLK	HCSL	100 MHz +/- 50 ppm constant clock. AC coupled output. Always on in the power-on state.
CPRSNT#	3.3 V Logic	Input with 1 kΩ pull-up resistor to 3.3 V. Not used.
CPERST#	3.3 V Logic	Open-drain output with 330 Ω pull-up resistor to 3.3 V.
CPWRON	3.3 V Logic	Open-drain output with 330 Ω pull-up resistor to 3.3 V. Always high in the power-on state.
CWAKE#	3.3 V Logic	Input with 1 kΩ pull-up resistor to 3.3 V. Not used.

Table 7-4 +3.3 V Power Specification

Description	Min.	Typ.	Max.	Unit
3.3 V Power Pins Voltage	3.0	3.3	3.6	V
3.3 V Power Pins Current	0	-	1.5	A

8 QSFP Interface

8.1 Description

The PFC is designed to operate with standard 40Gb/s QSFP AOCs supporting the Digital Diagnostic Monitoring (DDM) Interface. The PFC has 2 QSFP connectors compliant with the QSFP specification (AD-3). Due to the thermal constraints, the AOC power consumption must be less than 1.5 W. A typical AOC consumes less than 1 W. The AOC must be tested to verify reliable operation with the PCIe interface. The AOC vendors often change the AOC chipsets without issuing a Product Change Notification. Therefore the selected AOC must be version controlled in production. The list of tested cables is shown in Table 8-1.

Table 8-1. Tested AOC.

Manufacturer	Part Number	Description
Finisar	FCCN410QD3C10	Stable version.
Fiber Store	QSFP-AO10	Versions change often. Must be tested and version controlled.
10Gtek	AOC-Q1Q1-010	Versions change often. Must be tested and version controlled.

The QSFP1 and QSFP2 in the host PFC must be connected to the QSFP1 and QSFP2 in the target PFC respectively.

9 Configuration Interface

9.1 Description

The PFC operating mode and PCIe equalization settings are selected using the S1 and S2 DIP switches, respectively.

9.2 S1 DIP Switch

Table 9-1. S1 DIP Switch.

Switch	Description	Default
1	**PFC Mode:** OFF – Host ON – Target	OFF
2	**CPERST# Signals:** OFF – CPERST# is not generated ON – CPERST# is generated Note: The S1.2 settings must be the same in the host and target units.	OFF
3	Reserved	OFF
4	Reserved	OFF

9.3 S2 DIP Switch

The S2 DIP switch sets the equalization boost for the TX and RX lanes to compensate for losses in the PCIe cable. The default settings are highlighted.

Table 9-2. TX Lanes Equalization Settings.

S2.1	S2.2	S2.3	S2.4	TX Lanes EQ Boost (dB)	
				@ 4 GHz	@ 8 GHz
OFF	OFF	OFF	OFF	–0.3	–0.8
ON	OFF	OFF	OFF	0.4	1.3
OFF	ON	OFF	OFF	3.3	5.7
ON	ON	OFF	OFF	3.8	7.1
OFF	OFF	ON	OFF	4.9	8.4
ON	OFF	ON	OFF	5.2	9.1
OFF	ON	ON	OFF	5.4	9.8
ON	ON	ON	OFF	6.5	10.7
OFF	OFF	OFF	ON	6.7	11.3
ON	OFF	OFF	ON	7.7	12.6
OFF	ON	OFF	ON	8.7	13.6
ON	ON	OFF	ON	9.1	14.4
OFF	OFF	ON	ON	9.4	15.0
ON	OFF	ON	ON	10.3	15.9
OFF	ON	ON	ON	10.6	16.5
ON	ON	ON	ON	11.8	17.8

Table 9-3. RX Lanes Equalization Settings

S2.5	S2.6	S2.7	S2.8	RX Lanes EQ Boost (dB)	
				@ 4 GHz	@ 8 GHz
OFF	OFF	OFF	OFF	–0.3	–0.8
ON	OFF	OFF	OFF	0.4	1.3
OFF	ON	OFF	OFF	3.3	5.7
ON	ON	OFF	OFF	3.8	7.1
OFF	OFF	ON	OFF	4.9	8.4
ON	OFF	ON	OFF	5.2	9.1
OFF	ON	ON	OFF	5.4	9.8
ON	ON	ON	OFF	6.5	10.7
OFF	OFF	OFF	ON	6.7	11.3
ON	OFF	OFF	ON	7.7	12.6
OFF	ON	OFF	ON	8.7	13.6
ON	ON	OFF	ON	9.1	14.4
OFF	OFF	ON	ON	9.4	15.0
ON	OFF	ON	ON	10.3	15.9
OFF	ON	ON	ON	10.6	16.5
ON	ON	ON	ON	11.8	17.8

10 LED Indicators

10.1 Description

Table 10-1 LED Indicators

LED	Color	Description
PWR	Green	**Vin Power Indicator:** OFF – Vin is OFF Blinking, 0.5 sec ON, 0.5 sec OFF (1 Hz) – Vin is ON, and the PFC operates normally.
STS	Green	**Host PFC Status:** ON – Upstream CPWRON is high OFF – Upstream CPWRON is low **Target PFC Status:** ON – Downstream CPRSNT# is low OFF – Downstream CPRSNT# is high Note: The S1.1 DIP switch selects Host or Target Mode.
Q1	Green	**QSFP 1 Status:** The status is described in Table 10-2.
Q2	Green	**QSFP 2 Status:** The status is described in Table 10-2.

Table 10-2. QSFP Status.

QSFP LED	Description
OFF	QSFP is not present
Blinking, 0.25 sec ON, 0.25 sec OFF (2 Hz)	Received optical power is below the worst-case receiver sensitivity
ON	Optical transmitters and receivers are ON

11 Power Interface

11.1 Description

The PFC accepts 5-14 V DC, with a 12 V nominal power supply. The maximum power consumption of the PFC is 5.5 W. Maximum input current: 0.45 A @ 12 V.

The power consumption depends on the installed AOCs. A typical AOC consumes less than 1 W. In such a case, the PFC with 2 AOCs consumes 4.8 W.

If the 3.3 V power on the PCIe connector is used, then the maximum PFC input current must be increased accordingly, assuming 80 % efficiency of the internal PFC power supply.

11.2 PFC Power Connector Type

Type: DC Power Jack
Part Number: L721RA
Manufacturer: Switchcraft
Pin Assignment: Center Pin: +Vin, Sleeve Shunt: -Vin, Sleeve: -Vin

11.3 PFC Mating Power Connector Type

Type: DC Power Plug
Part Number: 767K or 768K
Manufacturer: Switchcraft
Pin Assignment: Tip Terminal: +Vin, Sleeve: -Vin

12 Thermal Interface

12.1 Description

The PFC operating temperature depends on the installed AOCs. The optical transceivers and cables are specified with a typical case temperature range from 0^0 to 70^0 C. The PFC operating case temperature range is a minimum of the QSFP operating temperature range and -40^0 to 85^0 C. The PFC temperature rise with typical AOCs is approximately 20^0. Ensure that the PFC enclosure surface temperature does not exceed the QSFP maximum allowed case temperature. Provide appropriate airflow or a thermal path to the environment if required. A thermal pad between the PFC and surface can be used if the PFC is mounted on a metal surface.