## Adnacom Inc.

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# Adnacom S31 64 Gb/s PCI Express Over Fiber Optic System

**User's Guide** 

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# 1 Terminology

Term	Description	
Add-in card	A card that is plugged into a connector and mounted in a chassis	
AOC	Active optical cable	
ATX	A system board form factor. Refer to the ATX Specification	
хN	A Link with "N" Lanes.	
DAC	Direct attach cable	
Downstream	The Ports on a Switch that are not the Upstream Port are Downstream Ports.	
EMI	Electromagnetic Interference	
ESD	Electrostatic Discharge	
Gb/s	Gigabit per second	
GT/s	Gigatransfers per second	
Gen 1	PCIe 2.5 GT/s	
Gen 2	PCIe 5 GT/s, backward compatible with Gen 1	
Gen 3	PCIe 8 GT/s, backward compatible with Gen 1 and Gen 2	
Lane	A set of differential signal pairs, one pair for transmission and one pair for	
	reception. A by-N Link is composed of N Lanes	
Link	The collection of two Ports and their interconnecting Lanes. A Link is a dual-	
	simplex communications path between two components.	
microATX	A system board form factor. Refer to the microATX Specification	
NC	Not connected	
OS	Operating system	
PCle	Interconnect standard for PCI Express cards	
Port	Logically, an interface between a component and a PCI Express Link	
QSFP	Quad Small Form-factor Pluggable	
PCle Switch	A device that connects two or more Ports to allow PCIe packets to be routed	
	from one Port to another	
RMA	Return Material Authorization	
Root Complex	A device that connects the processor and memory subsystem to the PCI	
	Express switches and devices	
Upstream	The Port on a Switch that is closest topologically to the Root Complex is the	
	Upstream Port	

Table 1-1. Common terms used in the user's guide.

## 2 Applicable and Reference Documents

## 2.1 Reference Documents

RD-1: H18 Datasheet. Adnacom Inc., <u>https://adnacom.com</u>. RD-2: R34 Datasheet. Adnacom Inc., <u>https://adnacom.com</u>.

## 2.2 Applicable Documents

AD-1: PCI Express Base Specification, Revision 3.0. PCI-SIG, http://www.pcisig.com.

AD-2: PCI Express Card Electromechanical Specification, Revision 3.0. PCI-SIG, http://www.pcisig.com.

AD-3: SFF-8436. QSFP+ 4x 10 Gb/s Pluggable Transceiver, Revision 4.9. SFF Committee.

AD-4: Design Guide for Desktop Platform Form Factors, Revision 002. Intel Corporation.

## **3** System Description

#### 3.1 Overview

The Adnacom S31 is a multi-lane PCI Express Gen 3 extension system. The system consists of the Adnacom-H18 host adapter and Adnacom-R34 backplane connected by one or two cables. The system can operate with one or two QSFP transceivers, active optical cables (AOCs), or direct attach cables (DACs). The system's diagrams are shown in Figure 3-1 and Figure 3-2.



#### Figure 3-2. H18 Two Ports x4.



The Adnacom S31 allows system integrators to operate PCIe cards at long distances from the location of the computer system via a fiber optic cable with a maximum throughput of 64 Gb/s. No additional host software drivers are required during installation or operation.

The R34 PCIe slots support bifurcation. The supported configurations are shown in Table 3-1 and Table 3-2.

Slot 1	Slot 2
1 port x4	1 port x4
1 port x8	Disabled
2 port x4	Disabled

### Table 3-1. S1 and S2 Slot Supported Configurations.

#### Table 3-2. S3 and S4 Slot Supported Configurations.

Slot 3	Slot 4
1 port x8	1 port x8
1 port x8	2 ports x4
1 port x16	Disabled
2 port x8	Disabled
2 ports x4	2 ports x4
4 ports x4	Disabled

The use of fiber optics provides electrical isolation and the ability to use long cables. The system integrators can use the system in applications where equipment operates in harsh environmental conditions or must be isolated from the host computer. The expansion system is transparent to software applications and drivers so that industry-standard desktop computers and servers can communicate with remote devices without additional programming.

#### 3.2 **Recommended Transceivers and Cables**

For information on tested cable lengths and measured data transfer rates, please visit the S31 product webpage: <u>https://adnacom/s31/</u>.

#### 3.2.1 Active Optical Cables

#### Table 3-3. Tested AOC.

Manufacturer	Part Number	Description
Finisar	FCCN410QD3C10	Reliable operation.
Fiber Store	QSFP-AO10	Reliable operation.
Others		Not all cables may work reliably. Adnacom recommends
		testing cables using the web interface described in
	section 10. The web interface helps to debug and identify	
		problems with the cable link.

## 3.2.2 Optical Transceivers

The S31 can operate with standard multi-mode and single-mode QSFP transceivers. The transceivers should consume less than 1.5 W to keep their temperature within recommended operating conditions. If transceivers consume more than 1.5 W, it is recommended to install heatsinks on the QSFP cages. The transceiver's power consumption and case temperature can be verified using the web interface described in section 9.

Manufacturer	Part Number	Description
Finisar	FTL4C1QL2C	Reliable operation.
Fiber Store	QSFP-LX4-40G	Reliable operation.
10Gtek	ALQ10-IR4-02	Reliable operation.
	ALQ10-LR4-10	

#### Table 3-4. Tested Transceivers.

### 3.2.3 LC-LC Cables

Multi-mode and single-mode LC-LC duplex cables can be used with single-mode QSFP transceivers with LC connectors. The QSFP transceivers multiplex and demultiplex 4 PCIe Gen 3 lanes into a single LC-LC duplex cable using Coarse Wavelength Division Multiplexing (CWDM). A single LC-LC duplex cable supports a 32 Gb/s data rate. The recommended multi-mode cable types are OM3 and OM4. The recommended maximum cable lengths for different cable types are shown in Table 3-5. The system performance depends on the cable length. For further information, visit https://adnacom.com/s31/.

#### Table 3-5. Recommended Maximum Length for LC-LC Cables.

Cable Type	Typical Length
Multi-Mode OM1 62.5/125 µm	40 m
Multi-Mode OM2 50/125 µm	100 m
Multi-Mode OM3 50/125 µm	350 m
Multi-Mode OM4 50/125 µm	550 m
Single-Mode OS1 9/125 µm	1 km
Single-Mode OS2 9/125 μm	1 km

#### 3.2.4 Direct Attach Cables

#### Table 3-6. Tested DAC.

Manufacturer	Part Number	Description
3M	9QA0-111-12-3.00	3 m passive cable.
Amphenol	10093084-5070LF	7 m passive cable.

## **4** System Operation

#### 4.1 Slot Configuration

The R34 slots can be configured using the S1.1 and S1.2 DIP switches or the web configuration page described in section 10.4.3. The type of configuration control is selected on the configuration page.

When the R34 is ON, the status LED D15 indicates the type of slot configuration:

- D15 is OFF: The slot configuration is controlled by the S1.1 and S1.2 DIP switches
- D15 is ON: The slot configuration is controlled by the settings on the configuration page described in section 10.4.3.

#### 4.1.1 Supported Configurations by DIP Switch

#### Table 4-1. S1 and S2 Slots Configurations.

S1.1	Slot 1	Slot 2
OFF	1 port x4	1 port x4
ON	1 port x8	Disabled

#### Table 4-2. S3 and S4 Slots Configurations.

S1.2	Slot 1	Slot 2
OFF	1 port x8	1 port x8
ON	1 port x16	Disabled

#### 4.1.2 Supported Configurations by Configuration Page

#### Table 4-3. S1 and S2 Slots Configurations.

Slot 1	Slot 2
1 port x4	1 port x4
1 port x8	Disabled
2 port x4	Disabled

#### Table 4-4. S3 and S4 Slots Configurations.

Slot 3	Slot 4
1 port x8	1 port x8
1 port x8	2 ports x4
1 port x16	Disabled
2 port x8	Disabled
2 ports x4	2 ports x4
4 ports x4	Disabled

#### 4.2 **Power Modes**

#### 4.2.1 S31 Power-ON/OFF Modes

The R34 can turn ON and OFF a standard computer power supply. The R34 can operate in one of three power control modes.

Mode	S1.3	S1.4	Description
1	OFF	OFF	Power ON and OFF is controlled by the momentary button
			SW6, or an external momentary switch connected to J9
			pins 2 and 4
2	ON	OFF	The power supply and R34 are always ON
			This mode is used with a custom power supply
3	OFF	ON	Power is turned ON and OFF automatically when the
			computer is turned ON and OFF

#### Table 4-5. R34 Power Control Modes.

Note: Disconnection of the fiber optic cable or cycling the power supply during operation requires a computer restart.

#### 4.2.2 Manual Power-ON/OFF Sequence (Modes 1 and 2)

#### **Power-On Sequence**

- Power on the R34.
- Power on the host computer.

#### **Power-Off Sequence**

- Power off the host computer.
- Power off the R34.

#### 4.2.3 Automatic Power-ON/OFF Sequence (Mode 3)

Mode 3 can be used only with an optical cable and a standard computer power supply or a power supply with a 5V standby voltage and a PS\_ON# signal. After installing the system, connect the power cord and switch ON the power switch on the R34 power supply to provide standby power to the R34. In this mode, the power sequence is controlled automatically. When the computer is turned ON or OFF, the R34 is turned ON or OFF automatically.

#### 4.3 Fan Configuration

The speed of the fans can be configured if the fans have the PWM control signal on the 4-wire connector. The fan profiles are selected on the configuration page described in section 10.4.3.

## **5** System Installation

### 5.1 Installation Recommendations

It is highly recommended to update your computer's BIOS and OS. The latest BIOS update and its installation instructions can be downloaded from the computer or motherboard manufacturer's website. If a BIOS update does not solve installation issues, further diagnostics may be required. The system may be installed on a different computer to verify Adnacom S31 functionality.



**ESD Warning:** The electronic parts are sensitive to electrostatic discharges. Please use an electrostatic wrist strap and/or conductive mat when executing the steps below.

#### 5.2 **Preparing Your Computer**

- The system does not support overclocking. Please make sure that the PCI Express clock frequency is set to either the default value or 100 MHz in the BIOS.
- The optical transceivers used in the system do not support PCI Express link power management. Therefore, it is recommended to disable all power management features on the computer. The step-by-step instructions for Windows 7, 8, and 10 can be found on the <u>https://adnacom.com/s31</u> page. For other operating systems, please consult your OS documentation, or if you need additional assistance, please contact the OS vendor.

#### 5.3 **Power Supply Minimum Load Requirements**

• The R34 backplane is designed to be powered by a standard computer power supply. Many computer power supplies require a minimum load to provide a stable output voltage and, in some cases, may not even turn on. If the installed add-in cards do not consume enough power for stable power supply operation, an additional load can be added by connecting chassis fans or a load resistor to the power supply.

#### 5.4 Installing H18 Host Adapter Card

- Power off the host computer and unplug its power cord.
- Remove the computer's cover.
- Identify any PCIe x8 or x16 slot on the motherboard.
- Configure the H18 using the DIP switch settings described in Table 7-2.
- Remove the metal bracket for the slot you have selected. Keep both the bracket cover and the retaining screw.
- Insert the H18 card into the identified PCIe slot by pushing gently on the card. Secure the card to the computer chassis using the retaining screw.
- There should be sufficient airflow to keep the PCIe switch temperature below the maximum limit. The temperature can be verified using the web interface described in section 10.
- Connect the power cord and verify that the red standby LED is ON when the computer is OFF. If the standby LED is OFF, it indicates that there is no +3.3Vaux voltage on the PCI slots. Check the BIOS settings to enable the voltage or reset the BIOS settings to the default values. In DELL computers, +3.3Vaux is enabled by setting BIOS Settings->Power Management-> Deep Sleep Control->Disabled.

#### 5.5 Installing R34 Backplane

- The R34 may be mounted in any microATX or ATX case.
- Connect the main power supply cable to the R34 J8 connector.
- Additional power may be supplied via the J10 and J11 connectors.
- If necessary, connect an additional load to the power supply as described in section 5.3.
- Set up the power control mode on the R34, as described in section 4.
- Configure the R34 using the DIP switch settings described in Table 8-1 or the configuration page described in section 10.4.3.
- There should be sufficient airflow to keep the PCIe switch temperature below the maximum limit. The temperature can be verified using the web interface described in section 10. If the installed fans have the PWM signal, then their profile can be selected on the configuration page described in section 10.4.3.

#### 5.6 Installing User's PCIe Cards into R34 Backplane

- Follow the recommendations and procedures provided by the card manufacturer for installation into standard computer slots.
- Install the user's cards into the J1–J4 slots on the R34. Ensure that the slots are enabled in the configuration selected by the S1.1 and S1.2 switches.

#### 5.7 Installing QSFP Transceivers and Connecting Fiber Optic Cables

- When the H18 is configured in the one-port x8 mode, the QSFP 1 must be connected. If the QSFP 2 is not used, it is recommended to remove the transceiver to prevent link training failure.
- When the H18 is configured in the two-port x4 mode, the QSFP 1 and QSFP 2 can be used in any combination.
- The QSFP 1 on the R34 must be connected. If QSFP 2 is not used, it is recommended to remove the transceiver to prevent link training failure.
- In the one-port x8 mode, both cables must have the same length and be of the same type.

H18 Cable Port	Number of QSFPs	Connection
One port x8	2	H18 QSFP 1 to R34 QSFP 1
	See Figure 5-1	H18 QSFP 2 to R34 QSFP 2
	1	H18 QSFP 1 to R34 QSFP 1
	See Figure 5-2	Unplug unused transceivers and cables from the
		QSFP 2 connectors on the H18 and R34.
Two ports x4	2	H18 QSFP 1 to R34 1 QSFP 1
	See Figure 5-3	H18 QSFP 2 to R34 2 QSFP 1
	1	H18 QSFP 1 to R34 QSFP 1 or
	See Figure 5-3	H18 QSFP 2 to R34 QSFP 1

#### Table 5-1. Valid Cable Connections.



### Figure 5-1. H18 One Cable Port x8 with Two Cables.







*Figure 5-3. H18 Two Cable Ports x4 with Two Cables.* 

#### 5.8 **Turning on the System for the First Time**

- Power on the system, as indicated in section 4.
- The system operating status can be verified using the web interface described in section 10.

## 6 System Functionality Verification

To verify a successful installation, use the **Device Manager**. In the **Device Manager**, click on the **View** menu and select **View Devices by Connection**.

### Figure 6-1. Device Manager.

To see if your installation is successful, click on the arrow to the left of the **ACPI** to open it, then within **PCI Bus**, check the lines containing the words "**PCI Express Root**" or "**PCI standard PCI-to-PCI bridge**." Under one of the lines, you should see multiple PCI-to-PCI bridges and your add-in card. Figure 6-2 Figure 6-2shows the H18 and R34 cards.



#### Figure 6-2. S31 System View in Device Manager.

Right-click on the "**PCI standard PCI-to-PCI bridge**" line you want to view, then click **Properties.** On the **Details** tab, you can verify a vendor and the device ID of the selected device.

All Adnacom H18 and R34 boards have the Vendor ID = 10B5. The H18 Device ID is 8718, and the R34 Device ID is 8734, as shown in Figure 6-3 and Figure 6-4, respectively.

PCI-to-PCI Bridge Properties	×
General Driver Details Events Resources	
PCIto-PCI Bridge	
Property	
Hardware Ids	$\sim$
Value	
PCI\VEN_10B5&DEV_8718&SUBSYS_871810B5&REV_AB PCI\VEN_10B5&DEV_8718&SUBSYS_871810B5 PCI\VEN_10B5&DEV_8718&CC_060400 PCI\VEN_10B5&DEV_8718&CC_0604	
OK Can	cel

#### Figure 6-3. H18 Hardware IDs.

PCI-to-PCI Bridge Properties	×
General Driver Details Events Resources	
PCIto-PCI Bridge	
Property	
Hardware Ids	$\sim$
Value	
PCI\VEN_10B5&DEV_8734&SUBSYS_873410B5&REV_AB PCI\VEN_10B5&DEV_8734&SUBSYS_873410B5 PCI\VEN_10B5&DEV_8734&CC_060400 PCI\VEN_10B5&DEV_8734&CC_0604	
OK Cano	cel

## Figure 6-4. R34 Hardware IDs.

If the installation was unsuccessful, please go to Troubleshooting section 11.

## 7 H18 PCIe Host Adapter

## 7.1 H18 Drawing



## 7.2 H18 Cable Interface

#### Table 7-1. H18 PCIe Cable Interface.

Number of Ports	Port Number	Port Width	PCIe Lanes	QSFP	QSFP TX/RX
	1	x8	0-3	1	1-4
I	1		4-7	2	1-4
2	1	x4	0-3	1	1-4
	2	x4	0-3	2	1-4
4	1	x2	0-1	1	1-2
	2	x2	0-1	L	3-4
	3	x2	0-1	2	1-2
	4	x2	0-1	2	3-4

## 7.3 H18 S1 DIP Switch Description

## Table 7-2. H18 DIP Switch.

Switch	Descriptio	n			Default
1	Cable Inte	rface Conf	iguration		OFF
2	S1.1	S1.2	Configuration		OFF
	OFF	OFF	1 port x8		
	ON	OFF	2 ports x4		
	OFF	ON	4 ports x2 (2 ports per QSFP)		
	ON	ON	Reserved		
	Note: 4 po	rts x2 conf	iguration is not used with the R34 back	plane.	

Switch	Description	Default
3	Gen 2 Cable Interface	OFF
	OFF – Gen 3	
	ON – Gen 2. Set for Gen 2 ports or to limit the cable interface speed	
4	Optical Reset	OFF
	OFF – disabled	
	ON – enabled. The lasers are turned OFF during the computer reset.	
	Note: Optical reset is not required for the R34 backplane.	
5	Hot Plug Enable	OFF
	OFF – Hot Plug is disabled	
	ON – Hot Plug is enabled	
6	Wake Enable	OFF
	OFF – Wake is disabled	
	ON – Wake is enabled	
7	Reserved	OFF
8	IP Configuration	
	OFF – Static IP address 198.168.100.101	OFF
	ON – User's IP Configuration described in section 10.2	

## 7.4 H18 LEDs Description

## Table 7-3. H18 LEDs.

LED	Color	Description
D1	Red	Standby Status:
		ON – standby mode
		OFF – the computer power supply is ON, or PCIe 3.3V AUX power is OFF
D2	Green	Computer Power Status:
		ON – the computer power supply is ON
		OFF – the computer power supply is OFF
D3	Red	Error Status: Reserved
D4		
D5	Green	Status:
D6		One and two ports configurations:
		Reserved
		Four ports configuration:
		D5 – Port 2 link status described in Table 7-4
		D6 – Port 4 link status described in Table 7-4
D7	Blue	Host Link Status: The status described in Table 7-4
D8	Green	QSFP 1 Status: The status described in Table 7-5
D9	Blue	Remote Link 1 Status: Port 1 link status described in Table 7-4
D10	Green	QSFP 2 Status: The status described in Table 7-5

LED	Color	Description
D11	Blue	Remote Link 2 Status:
		One port configuration:
		The status is the same as the Remote Link 1 status if QSFP 2 is connected to the
		remote device
		Two ports configuration:
		Port 2 link status described in Table 7-4
		Four ports configuration:
		Port 3 link status described in Table 7-4

## Table 7-4. PCIe Link Status.

PCIe Link LED	Description
OFF	Link is Down
Blinking, 0.5 sec ON, 0.5 sec OFF (1 Hz)	Link is Up, 2.5.0 GT/s
Blinking, 0.25 sec ON, 0.25 sec OFF (2 Hz)	Link is Up, 5.0 GT/s
ON	Link is UP, 8.0 GT/s

#### Table 7-5. QSFP Status.

QSFP LED	Description
OFF	QSFP is not powered
Blinking, 0.25 sec ON, 0.25 sec OFF (2 Hz)	Received optical power is below the worst-case
	receiver sensitivity
ON	Transmitter and receiver are ON

## 7.5 H18 Connectors Description

## Table 7-6. H18 Connectors.

Designator	Description
J1	QSFP 1 connector
J2	QSFP 2 connector
J3	Ethernet connector
J4	Test connector. Factory only.

# 8 R34 PCIe Backplane

## 8.1 R34 Drawing

Figure 8-1. R34 Drawing.



## 8.2 R34 S1 DIP Switch Description

Switch	Description	on					Default
1	Slots 1 and 2 Configurations Controlled by S1.1 DIP switch			OFF			
	S1.1	S	lot 1	Slot	2		
	OFF	1 p	ort x4 1 port x4		t x4		
	ON	1 p	ort x8	Disab	led		
	Slots 1 ar	nd 2 Co	onfigurat	tions Cor	ntrolled	by Configuration Page	
	Slot	1	Slo	ot 2			
	1 port	t x4	1 pc	ort x4			
	1 port	t x8	Disa	bled			
	2 port	t x4	Disa	bled			
	The config	guratio	n page is	describe	d in see	ction 10.4.3	
2	Slots 3 ar	nd 4 Co	onfigurat	ions Cor	ntrolled	by S1.2 DIP switch	OFF
	<b>S1.2</b>	S	lot 3	Slo	t 4		
	OFF	1 p	oort x8	1 poi	rt x8		
	ON	1 p	ort x16	Disal	oled		
	Slots 2 ar	nd 3 Co	onfigurat	tions Cor	ntrolled	by Configuration Page	
	Slot	3	Slo	ot 4			
	1 port	t x8	1 pc	ort x8			
	1 port	t x8	2 ро	rts x4			
	1 port	x16	Disa	bled			
	2 port	t x8	Disa	bled			
	2 port	s x4	2 ро	rts x4			
	4 port	s x4	Disa	bled			
	The configuration page is described in section 10.4.3						
3	R34 Powe	er Cont	trol				OFF
4	<b>S1.3</b>	<b>S1.4</b>			D	Description	OFF
	OFF	OFF	Power C	DN/OFF c	ontrolle	ed by the power button on R34	
	ON	OFF	Power is always ON				
	OFF	ON	Power is turned ON and OFF automatically when the				
			computer is turned ON and OFF				
	ON	ON	Reserved				
5	Hot Plug Enable OFF						
	OFF – Hot Plug is disabled						
	ON – Hot	Plug is	enabled				
6	Wake Enable   OFF						
	OFF – Wake is disabled						
	ON – Wak	ke is en	abled				077
/	Reserved	- •					OFF
8	IP Config	uratio	<b>n</b>	0 4 6 0 4 5	0.4.00		077
	OFF – Stat	tic IP ac	dress 19	8.168.100	J.102		OFF
	ON – User's IP Configuration described in section 10.2						

#### Table 8-1. R34 DIP Switch.

LED	Color	Description
D1	Green	Slot 1 Power Indicator: Status described in Table 8-3
D2	Yellow	Slot 1 Attention Indicator: Status described in Table 8-4
D3	Blue	Slot 1 Link Status: Status described in Table 7-4.
		If the slot is split into two ports, the status is shown for the port connected to the
		least significant lanes.
D4	Green	Slot 2 Power Indicator: Status described in Table 8-3
D5	Yellow	Slot 2 Attention Indicator: Status described in Table 8-4
D6	Blue	Slot 2 Link Status: The status described in Table 7-4
D7	Green	Slot 3 Power Indicator: Status described in Table 8-3
D8	Yellow	Slot 3 Attention Indicator: Status described in Table 8-4
D9	Blue	Slot 3 Link Status: Status described in Table 7-4.
		If the slot is split into two or four ports, the status is shown for the port
		connected to the least significant lanes. Use the web interface to see the status
		of other ports.
D10	Green	Slot 4 Power Indicator: Status described in Table 8-3
D11	Yellow	Slot 4 Attention Indicator: Status described in Table 8-4
D12	Blue	Slot 4 Link Status: The status described in Table 7-4
		If the slot is split into two ports, the status is shown for the port connected to the
		least significant lanes. Use the web interface to see the status of other ports.
D13	Red	Error Status:
D14		Reserved
D15	Green	Slot Configuration:
		OFF – Slots configured by S1.1 and S1.2 DIP switches
	_	ON – Slots configured via the web interface described in section 10.4.3
D16	Green	Operating Status:
D17		Reserved
D18		
D19	Blue	Host Link Status: The status described in Table 7-4
D20	Green	QSFP 1 Status: The status described in Table 7-5
D21	Green	QSFP 2 Status: The status described in Table 7-5
D22	Green	Power On
		OFF – the main power supply is OFF, or 5VSB is OFF
		ON – the main power supply is ON
D23	Red	Standby Status:
		ON – standby mode
		OFF – the main power supply is ON, or the 5VSB is OFF
D24	Red	Power Failure:
		OFF = +3.3V, $+12V$ are within the regulation thresholds
	D - J	ON – one or both +3.3V and +12V power supplies failed
D25	Ked	Keset Status:
		UFF – reset is de-asserted
		ON – reset is asserted

#### Table 8-2. R34 LEDs.

#### Table 8-3. Power Indicator Status.

Power LED	Description
OFF	All supply voltages (except 3.3Vaux) have been removed from the slot. Insertion or
	removal of add-in cards is permitted.
ON	The slot is powered ON. Insertion or removal of add-in cards is not permitted.
Blinking	The slot is in the process of powering up or down. Insertion or removal of add-in
	cards is not permitted.

#### Table 8-4. Attention Indicator Status.

Attention LED	Description
OFF	Normal - Normal operation
ON	Attention - Operational problem at this slot
Blinking	The slot is being identified at the user's request

## 8.4 R34 Buttons Description

#### Table 8-5. R34 Buttons.

Switch	Description
SW1	Slot 1 attention button
SW2	Slot 2 attention button
SW3	Slot 3 attention button
SW4	Slot 4 attention button
SW4	Reset button
SW4	Power button

## 8.5 R34 Connectors Description

## Table 8-6. R34 Connectors.

Designator	Description
CON1	QSFP 1 connector
CON2	QSFP 2 connector
J1	PCle slot configured x4 or x8
J2	PCle slot configured x4 or disabled if J1 is configured x8
J3	PCle slot configured x8 or x16
J4	PCle slot configured x8 or disabled if J3 is configured x16
J5	Test connector. Factory only.
J6	Ethernet connector
J7	Test connector. Factory only.
J8	ATX Main Power Connector 24 pin
J9	Front panel connector
J10	EPS/ATX12V 8 pin
J11	EPS/ATX12V 8 pin
J12	Fan connector
J13	Fan connector
J14	Fan connector
J15	Fan connector

Pin	Signal Name	Pin	Signal Name
1	+3.3VDC	13	+3.3VDC
2	+3.3VDC	14	NC
3	GND	15	GND
4	NC	16	PS_ON#
5	GND	17	GND
6	+5VDC	18	GND
7	GND	19	GND
8	PWR_OK	20	NC
9	+5VSB	21	NC
10	+12VDC	22	NC
11	+12VDC	23	NC
12	+3.3VDC	24	GND

### Table 8-7. J8 Main Power Connector.

## Table 8-8. J10 and J11 Power Connectors.

Pin	Signal Name	Pin	Signal Name
1	GND	5	+12VDC
2	GND	6	+12VDC
3	GND	7	+12VDC
4	GND	8	+12VDC

#### Table 8-9. J12, J13, J14 and J15 Fan Connectors.

Pin	Signal Name	
1	GND	
2	+12 V	
3	Tachometer	
4	PWM Control	

Pin	Signal Name
1	Reset Switch
3	Reset Switch
2	Power ON/OFF Switch
4	Power ON/OFF Switch
5	GND
6	GND
7	Standby LED (-)
9	Stand-by LED (+)
8	Power ON LED (-)
10	Power ON LED (+)

#### Table 8-10. R34 J9 Front Panel Header.





## 9 Custom Power Supply

#### 9.1 **Power Supply Requirements**

The power supply voltages must remain within the regulation ranges shown in Table 9-1 and Table 9-2 when measured at the power connector on the R34 board under all line, load, and environmental conditions. The R34 power connector pinout is described in Table 8-7.

Output	Range	Min	Nom	Мах	Unit
+3.3V	+/-5%	+3.14	+3.30	+3.47	V
+12V	+/-5%	+11.40	+12.00	+12.60	V
+5VSB	+/-5%	+4.75	+5.00	+5.25	V

## Table 9-2. DC Output Noise/Ripple.

Output	Maximum Ripple and Noise (mVp-p)
+3.3V	50
+12V	120
+5VSB	50

There is no specific requirement for power supply sequencing of each of the power supply outputs. They may come up or go down in any order.

It is recommended to use the R34 web interface to measure the R34 power consumption with a standard power supply before designing a custom power supply.

#### 9.2 +5VSB Power Supply

+5VSB (pin 9) can be powered from a 12V power supply.

The +5VSB standby voltage is used if the custom power supply has an ON/OFF control input similar to the PS\_ON# signal in a standard computer power supply.

If a 5V power supply is not available, the R34 can be powered by 3.3V and 12V power supplies. In such a case, +5VSB must be connected to the +12V power supply.

The +5VSB power is used to power the R34 management controller and generate the +3.3Vaux voltages on the PCIe connectors.

#### 9.3 PS\_ON# Signal

The PS\_ON# (pin 16) is an open drain output with a 1K pull-up resistor to +3.3V. The output is 5V tolerant, so it can be pulled up to +5V by an external resistor. This pin can be left unconnected if the PS\_ON# signal is not used. If the power supply does not have the PS\_ON# input, the R34 must be configured in power control mode 2 by setting S1.3=ON and S1.4=OFF, as described in section 4.2.

#### 9.4 PWR\_OK Signal

The PWR\_OK (pin 8) input is a "power good" signal. It should be asserted high by the power supply to indicate that the +12V, +5V, and +3.3V power supplies are within the regulation ranges shown in Table 9-1. This pin can be left unconnected if the PWR\_OK signal is not available. The PWR\_OK input is 5V tolerant and pulled up to +3.3V by a 4.7K resistor on the R34.

#### 9.5 **Connection Diagrams**



## **10 Web Interface**

#### 10.1 Overview

The H18 and R34 have Ethernet connectors used to connect to the embedded web servers via standard Ethernet cables. The web interface allows monitoring of the board status, provides diagnostic information if problems occur, and is used to upgrade the firmware. The IP addresses can be static default, static user-programmable, or assigned by a DHCP server. The computer network adapter configuration for the default IP address is shown in Figure 10-1.

Internet Protocol Version 4 (TCP/IPv4)	Properties	$\times$
General		
You can get IP settings assigned auton this capability. Otherwise, you need to for the appropriate IP settings.	natically if your network supports ask your network administrator	
Obtain an IP address automatical	У	
Use the following IP address:		
IP address:	192 . 168 . 100 . 100	
Subnet mask:	255.255.255.0	
Default gateway:		
Obtain DNS server address autom	natically	
Use the following DNS server add	resses:	
Preferred DNS server:		
Alternate DNS server:		
Validate settings upon exit	Advanced	
	OK Cancel	

#### **10.2 IP Address Configuration**

The H18 and R34 IP addresses can be changed to operate on a user's network.

#### 10.2.1 Default IP Address: S1.8 = OFF

The default static IP address is selected by setting S1.8 = OFF.

- H18 IP Address: 192.168.100.101
- R34 IP Address: 192.168.100.102

#### 10.2.2 User's IP Address: S1.8 = ON

The user's configuration is selected by setting S1.8 = ON and configuring the IP settings via the Network Configuration page shown in Figure 10-2. The user's IP address can be static or assigned by a DHCP server. When the DHCP server assigns the IP address, the website is accessed using the programmed DHCP hostname; for instance, <u>http://ADNACOM-R34</u>. The DHCP name is not case-sensitive.

## Figure 10-2. IP Address Configuration.

Status	Network Conf	iguration	Firmware Update	Help
The S1.8 DIP switch se S1.8=OFF: Static IP 198 S1.8=ON: User's IP Cor	elects the network configuration 3.168.100.102 Ifiguration	on:		
User's IP Configuration	n:			
Obtain IP address at	utomatically:			
DHCP host name	: ADNACOM-R34			
$\bigcirc$ Use the following IP	configuration:			
IP Address:	192.168.100.102			
Subnet mask:	255.255.255.0			
Default gateway:	192.168.100.102			
Save Configuration				

#### 10.3 H18 Web Site IP: 192.168.100.101

#### 10.3.1 Overview

The website consists of 4 pages: Status, Network Configuration, Firmware Upgrade, and Help, as shown in Figure 10-3.

#### Figure 10-3. H18 Web Site.

								A	dna	CO	m	H18	}				
		Stati	us		^	Vetu	vork	Confi	gurat	ion	F	irmwai	re Upd	ate		Help	)
CONFI	GUR	ATIO	N														
HW R	ev	FW Re	v	Serial I	lumbe	er	PCIe S	witch									
000-0	0	3.1.1	40	C-0A-3D	-00-10	0-00	PEX8	718									
DIP Sw	itch																
<b>S1</b>	<b>S</b> 2	<b>S</b> 3	<b>S4</b>	<b>S</b> 5	<b>S6</b>	S7	<b>S8</b>										
OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF										
QSFP																	
QSFP	Pr	esent	Port	PCI	e Lane	es 👘	Vend	or	Part Nu	mber	Ser	ial Numbe	r Tech	nology			
2	-	Yes	1		4-7	FI	NISAR	CORP	FCCN410C	2D3C10 2D3C10		WORAA56	850 nr	n VCSEL			
										-							
Cable Port	Ma	c Speed	d Ma	ax Widt	'n												
1	T Tel	Gen3		8													
<b>.</b>																	
Port	Ma	c Spee	d Ma	ax Widt	:h												
0		Gen3		x8													
STATU Cable	s						_			_							
Port 1	Un	k Sp Ge	eed en3	width x8	Lini	k Up ms	ON	te Rei	.021 s	Reco	overy	Rx Error	Bad IL	P Bad D	LL Widt	n Retrain	Link Down
-											-	, ,					
Comput	er	/ En	ood	Width	-												
0	Up	K SP Ge	eeu en3	×8	-												
<b>D</b>		•			_												
Powe	g Sta	tus Time	Si	nce Res	et F	Reset	Rese	t Lenath	PCIe	Enum	Time						
Good	0	0:01:34	4 (	0:01:3	4	1	5	09 ms	3	0.043 s	5						
H18																	
Time	e	State	ТР	EX T	CPU	V +1	2V ]	+12V	V +3.3V	aux	I +3.3	BVaux					
00:02:	28	ON	42°	C 2	7° C	11.94	4 V 🛛 🗘	.601 A	3.28	V	0.14	10 A					
OSFP																	
QSFP	Po	wer	State	Тх	Rx	Lo	S Coun	t Tem	p Vcc	:	Icc	Rx1	Rx2	Rx3	Rx4	Start-Up	I2C Error
1	3	.3V	ON	ON	Good	1	0	23°	C 3.35	V 0.	197 A	737 µW	668 µW	668 µW	676 µW	447 ms	0
2	3	.3V	ON	ON	Good	1	0	23°	C 3.35	V 0.	201 A	661 µW	655 µW	655 µW	679 µW	448 ms	0
H18 Po	wer s	Supplie	s														
3.3V	Q	SFP1 3	.3V	QSFP2	3.3V	CPU	1.8V	PEX 1.	8V PEX	<b>CO.9V</b>	PEX	0.9VA					
3.3/V		3.35 \	/	3.35	v	1.,	9 V	1.//	v 0.	.90 V	0.	.90 V					

#### 10.3.2 Status Page

#### 10.3.2.1 Configuration

#### Table 10-1. Board Information.

Field	Description
HW REV	The board assembly revision
FW REV	The board firmware revision
Serial Number	The serial number of the board used in the PCIe switch configuration space and as the MAC address

Field	Description
PCle Switch	PEX8718 – PCIe switch part number

#### Table 10-2. DIP Switch.

Field	Description
S1-S8	The DIP switch status

#### Table 10-3. QSFP Configuration.

Field	Description
QSFP	The QSFP number on the board
Present	The presence status
Port	The PCIe switch port number connected to the QSFP
PCIe Lanes	The PCIe lane numbers connected to the QSFP
Vendor	The QSFP vendor name
Part Number	The QSFP part number
Serial Number	The QSFP serial number
Technology	The QSFP technology as defined in the QSFP specification.

## Table 10-4. Cable Interface Configuration.

Field	Description
Port	The PCIe switch port number connected to the QSFP
Max Speed	The maximum speed supported by the H18
Max Width	The maximum width supported by the H18. The width depends on the
	number of installed QSFPs.

## Table 10-5. Computer Interface Configuration.

Field	Description
Port	The PCIe switch port number connected to the PCIe slot
Max Speed	The maximum speed supported by the H18
Max Width	The maximum width supported by the H18.

#### 10.3.2.2 Status

## Table 10-6. Cable Interface Status.

Field	Description
Port	The PCIe switch port number connected to the QSFP
Link	The link status
Speed	The negotiated speed
Width	The negotiated width
Link Up	The time from the reset de-assertion to link up
Remote	The remote device status. Valid only for optical cables
Remote Up	The time from the reset de-assertion to remote ON. The remote should be
	ON before the PCIe enumeration starts. Otherwise, the remote will not be
	visible by the computer.
Recovery	The recovery state counter. The counter is used to evaluate the link quality.
	It should not count during the operation. A slow increment is acceptable.

Field	Description
Rx Error	The receiver error counter. The counter is used to evaluate the link quality. It
	should not change during the operation. A slow increment is acceptable.
Bad TLP	The bad TLP counter. The counter is used to evaluate the link quality. It
	should not change during the operation. A slow increment is acceptable.
Bad DLL	The bad DLL counter. The counter is used to evaluate the link quality. It
	should not change during the operation. A slow increment is acceptable.
Width Retrain	The number of times the H18 tried to retrain the link to the maximum
	width. The link must train before the PCIe enumeration starts.
Link Down	The link down counter. The counter shows how many times the link went
	down after restart. If the link is down, it requires either the computer restart
	or PCIe bus rescan to resume the operation.

## Table 10-7. Computer Interface Status.

Field	Description
Port	The PCIe switch port number connected to the PCIe slot
Link	The link status
Speed	The negotiated speed
Width	The negotiated width

## Table 10-8. Running Status.

Field	Description
Power	The power supply status
Time	The time since the computer power-up
Since Reset	The time since the last reset
Reset	The number of resets since the computer power-up
Reset Length	The length of the last reset pulse
PCIe Enum Time	The time from the last reset to the start of the PCIe switch enumeration.
	This time must be longer than the time required to turn on the remote
	device.

## Table 10-9. H18 Status.

Field	Description
Time	The elapsed time from powering the H18 in the computer slot by the
	+3.3Vaux voltage
State	The H18 state
T PEX	The PCIe switch junction temperature. The maximum operating junction
	temperature is 110° C.
T CPU	The junction temperature of the supervisory CPU. Maximum Tj = $125^{\circ}$ C
V +12V	The +12V slot voltage
I +12V	The +12V slot current
V +3.3Vaux	The +3.3Vaux slot voltage
I +3.3Vaux	The +3.3Vaux slot current

## Table 10-10. QSFP Status.

Field	Description
QSFP	The QSFP number on the board

Field	Description
Power	The power supply type powering the QSFP
State	The QSFP state
Tx	The transmitter status
Rx	The receiver status
LoS Counter	The Loss of Signal counter from the last reset
Temp	The internal QSFP temperature
Vcc	The internal QSFP voltage
lcc	The QSFP current
Rx1-Rx4	The measured Rx power
Start-Up	The QSFP initialization time
I2C Error	The number of I2C errors since the last reset

## Table 10-11. H18 Internal Power Supplies.

Field	Description
3.3V	The 3.3V power supply voltage
QSFP1 3.3V	The QSFP 1 3.3V power supply voltage measured on the connector
QSFP2 3.3V	The QSFP 2 3.3V power supply voltage measured on the connector
CPU 1.8V	The CPU 1.8V power supply voltage
PEX 1.8V	The PCIe switch 1.8V power supply voltage
PEX 0.9V	The PCIe switch digital 0.9V power supply voltage
PEX 0.9VA	The PCIe switch analog 0.9V power supply voltage

#### 10.4 R34 Web Site IP: 192.168.100.102

#### 10.4.1 Overview

The website consists of 5 pages: Status, Backplane Configuration, Network Configuration, Firmware Upgrade, and Help, as shown in Figure 10-4.

Figure	10-4.	R34	Web	Site.

								Adı	nac	om	<b>R34</b>			
	Sta	tus			L Co	Backpl nfigur	ane ation		Net Config	work juratio	n	Firmv	vare Upda	nte
ONFI	GURAT	ION												
HW Re	ev FV	/ Rev	Ser	rial Num	ber	PCIe Sw	itch							
031-0	1 3	.2.1	4C-0/	4-3D-06-	20-01	PEX873	4							
IP Swi	itch													
S1	S2	<b>S</b> 3	S4	S5 S	6 S	7 S8								
)++	OFF	OFF	OFF	OFF 0		FF OFF								
FP														
SFP	Prese	ent I	Port	PCIe La	nes	Vendor	P	art Number	Seria	Number	Techno	ology		
2	Yes		0	4-7		FINISAR CO	RP FC	CN410QD3C10	wo	RAASB	850 nm	VCSEL		
		_	-	. /										
ble	May C	need	Max	Midth										
0	Max S G	en3	max x	8										
ots	DCTo I	2005	Bort	Max 6	nood	Max Wid	th							
1	0-:	anes 3	1	Ge	n3	×4	u							
2	0-3	3	2	Ge	n3	x4								
3	0-1	7	4	Ge	n3	×8	_							
4	0-	/	5	Ge	n3	X8								
TATU able	S													
Port	Link	Spee	d Wi	dth R	ecover	y Rx Er	or Ba	d TLP Bad	DLL					
0	Up	Gena	; ,	(8	1	0		0 0						
ots														
ots Slot	PCIe L	anes	Port	Card	Link	Speed	Width	V +12V	I +12V	V +3.3V	I +3.3V	/ V +3.3	/aux I +3.3\	aux
ots Slot 1	PCIe L 0-:	anes 3	Port	Card Yes	Link Up	Speed Gen3	Width x2 x4	V +12V 11.78 V	I +12V 0.010 A 0.195 A	V +3.3V 3.36 V	I +3.3V	V +3.3V	V 115.00	mA nA
ilot 1 2 3	PCIe L 0-: 0-:	<b>anes</b> 3 3 7	Port 1 2 4	Card Yes Yes Yes	Link Up Up Up	Speed Gen3 Gen2 Gen3	Width x2 x4 x8	V +12V 11.78 V 11.78 V 11.78 V	I +12V 0.010 A 0.196 A 0.437 A	V +3.3V 3.36 V 3.36 V 3.35 V	I +3.3V 0.117 A 0.000 A 0.000 A	V +3.3V 3.31 3.31 3.31	/aux         I +3.3V           V         115.00           V         0.00 r           V         116.00	mA mA mA
ots lot 1 2 3 4	PCIe L 0-: 0-: 0-:	<b>anes</b> 3 3 7 7	Port 1 2 4 5	Card Yes Yes Yes No	Link Up Up Up	Speed Gen3 Gen2 Gen3	Width x2 x4 x8 -	V +12V 11.78 V 11.78 V 11.78 V 11.78 V	I +12V 0.010 A 0.196 A 0.437 A 0.000 A	V +3.3V 3.36 V 3.36 V 3.35 V 3.36 V	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A	V +3.3V 3.31 3.31 3.31 3.31 3.31 3.31	Yaux         I +3.3 V           V         115.00           V         0.00 r           V         116.00           V         0.00 r	mA nA mA nA
ots Slot 1 2 3 4	PCIe L 0-: 0-: 0-: 0-: 0-:	anes 3 3 7 7	Port 1 2 4 5	Card Yes Yes Yes No	Link Up Up -	Speed Gen3 Gen2 Gen3	Width x2 x4 x8 -	V +12V 11.78 V 11.78 V 11.78 V 11.78 V	I +12V 0.010 A 0.196 A 0.437 A 0.000 A	V +3.3V 3.36 V 3.36 V 3.35 V 3.36 V	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A	V +3.3V 3.31 3.31 3.31 3.31 3.31 3.31	Vaux         I +3.3V           V         115.00           V         0.00 r           V         116.00           V         0.00 r	mA nA mA nA
ots Slot 1 2 3 4 4	PCIe L 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-:	anes 3 7 7 7 7 8 7	Port 1 2 4 5	Card Yes Yes Yes No	Link Up Up -	Speed Gen3 Gen2 Gen3 -	Width x2 x4 x8 - set Re	V +12V 11.78 V 11.78 V 11.78 V 11.78 V 11.78 V	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En	V +3.3V 3.36 V 3.35 V 3.35 V 3.36 V	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A	V +3.3V 3.31 3.31 3.31 3.31 3.31 3.31	Vaux         I +3.3V           V         115.00           V         0.00 r           V         116.00           V         0.00 r	mA nA mA nA
nts lot 1 2 3 4 4 nning Good	PCIe L 0-: 0-: 0-: 0-: 0-: 9 Status 7 Pow 29	anes 3 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	Port 1 2 4 5 Tir 00:0	Card           Yes           Yes           Yes           No           me         \$           7:09	Link Up Up -	Speed           Gen3           Gen2           Gen3           -	Width x2 x4 x8 - set Re	V +12V 11.78 V 11.78 V 11.78 V 11.78 V 11.78 V seet Length 102 ms	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En 36.0	V +3.3V 3.36 V 3.36 V 3.35 V 3.36 V um Time D11 s	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A	V +3.3V 3.31 3.31 3.31 3.31 3.31 3.31 3.31	Vaux         I +3.3V           V         115.00           V         0.00 r           V         116.00           V         0.00 r	mA nA mA nA
ots Slot 1 2 3 4 4 Power Good	PCIe L 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-:	anes 3 7 7 7 9 7 9 7 9 7 9 7 9 7 9 7 9 7 9 7	Port 1 2 4 5 Tin 00:0	Card           Yes           Yes           Yes           No           me         \$           7:09	Link Up Up -	Speed           Gen3           Gen2           Gen3           -	Width x2 x4 x8 - set Re	V +12V 11.78 V 11.78 V 11.78 V 11.78 V 11.78 V 11.78 V set Length 102 ms	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En 36.0	V +3.3V 3.36 V 3.36 V 3.35 V 3.35 V 3.36 V um Time D11 s	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A	/ V +3.31 3.31 3.31 3.31 3.31 3.31 3.31	Yaux         I +3.3V           V         115.00           V         0.00 r           V         116.00           V         0.00 r	mA nA mA nA
lots Slot 1 2 3 4 4 Power Good 34 Time	PCIe L 0-: 0-: 0-: 9 Status 9 S	anes 3 7 7 7 7 7 7 7 7 7 7 7 7 7	Port 1 2 4 5 Tin 00:0	Card           Yes           Yes           No           ne         \$           7:09           T CPU	Link Up Up -	Speed Gen3 Gen2 Gen3 sos sos sos Sos Sos Sos Sos Sos Sos Sos	Width X2 X4 X8 - set Re 1 T US	V +12V           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           10.2 ms	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En 36.0 V +12V	V +3.3V 3.36 V 3.36 V 3.35 V 3.35 V 3.36 V Um Time D11 s I +12V	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A	<ul> <li>V +3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>V I +3.31</li> </ul>	/aux         I +3.3\           V         115.00           V         0.00 r           V         116.00           V         0.00 r           V         116.00           V         0.00 r	mA nA mA nA nA
lots           Slot           1           2           3           4           unning           Power           Good           34           Time           00:27:	PCIe L 0-: 0-: 0-: 9 Status 7 Pow 29 29 29 242 (0)	anes 3 7 7 7 9 9 9 9 9 9 9 9 9 9 9 9 9	Port 1 2 4 5 Tir 00:0 T PEX 59° C	Card           Yes           Yes           No           me         \$           7:09           T CPU           31° C	Link Up Up - Since R 00:07 T U 33°	Speed           Gen3           Gen2           Gen3           seset           Re           89           T U9           ° C	Width           x2           x4           x8           -           set         Re           1         T US           2         30°	V +12V           11.78 V           11.79 V           102 ms           102 ms           102 ms           102 ms	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En 36.0 V +12V 11.78 V	V +3.3V 3.36 V 3.36 V 3.35 V 3.36 V um Time D11 s I +12V 0.769 A	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A V +3.3' 3.36 V	<ul> <li>V +3.3\ 3.31         3</li></ul>	/aux I +3.33 ∨ 115.00 ∨ 0.00 r ∨ 116.00 ∨ 0.00 r √ V +5VSB A 5.05 ∨	mA mA mA mA nA
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ots Slot 1 2 3 4 Vunning Power Good 34 Time 00:27: SFP QSFP	PCIe L 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-:	anes 3 3 7 7 rer Up 1 ms cate DN	Port 1 2 4 5 Tin 00:0 T PEX 59° C	Card           Yes           Yes           No           me         1           7:09           T CPU           31° C           Tx         R	Link Up Up - Since R 00:07 33° X L	Speed           Gen3           Gen4           Gen3           Gen3	Width           x2           x4           x8           -           set         Re           1         T US           2         30°           r         Tem	V + 12V           11.78 V           11.78 V           11.78 V           11.78 V           11.78 V           11.78 V           102 ms           C           29° C           p           Vcc	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En 36.0 V +12V 11.78 V Icc	V +3.3V 3.36 V 3.36 V 3.35 V 3.36 V um Time D11 s I +12V 0.769 A Rx1	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A V +3.31 3.36 V Rx2	<ul> <li>V +3.3\ 3.31         3.31         3.31         3.31         3.31         3.31         3.31         0.396         A         Rx3         </li> </ul>	/aux         I + 3.33           V         115.00           V         0.00 r           V         116.00           V         116.00           V         0.00 r           V         116.00           V         5.05 V           Rx4         Stat	mA mA mA mA nA I +5V 0.349
lots Slot 1 2 3 4 unning Power Good 34 Time 00:27: SFP QSFP 1 2	PCIe L 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-:	anes 3 7 7 7 7 7 7 7 7 7 7 7 7 7	Port 1 2 4 5 Tit 00:0 TPEX 59° C tate DN 0	Card           Yes           Yes           No           me         \$           7:09           T CPU           31° C           Tx         R           ON         Go	Link Up Up Up Since R 00:07: 33° x L od	Speed           Gen3           Gen2           Gen3           -           eset         Re           08           89         T U9           0         31°           o         0	Width           x2           x4           x8           -           sset         Re           1         T US           2         30°           r         Tem           35° (           2770'	V + 12V           11.78 V           11.78 V           11.78 V           11.78 V           11.78 V           102 ms           C           29° C           P           Vcc           C           232 V	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En 36.0 V +12V 11.78 V Icc 0.195 A	V +3.3V 3.36 V 3.36 V 3.35 V 3.36 V um Time D11 s I +12V 0.769 A Rx1 757 µW	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A 0.000 A V +3.31 3.36 V Rx2 706 µV	<ul> <li>V +3.33</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>0.31</li> <li>0.396 A</li> <li>Rx3</li> <li>706 µW</li> <li>655 rW</li> </ul>	/aux         I + 3.33           // V         115.00           V         0.00 r           V         116.00           V         116.00           V         116.00           V         0.00 r           J         4.505 V           Rx4         Sta           722 µW         45           674 µW         45	mA mA mA mA nA I +5V 0.349
ots Slot 1 2 3 4 Unning Power Good 34 Time 00:27: SFP QSFP 1 2	PCIe L 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-:	anes 3 3 7 7 7 8 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9 9	Port           1           2           4           5             Tin           00:0         T PEX           59° C         Cate	Card           Yes           Yes           No           me         \$           7:09           T CPU           31° C           TX         R           ON         Go	Link Up Up Up Up Up Up Up V Up Up Up Up Up Up Up Up Up Up	Speed           Gen3           Gen2           Gen3           -           eset         Re           08           89         T U9           0         31°           os Counte         0           0         0	Width           x2           x4           x8           -           set         Re           1         T U92           2         30°           r         Tem           35° (         37° (	V + 12V           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           102 ms           01 T U92           C           29° C           P Vcc           C           3.32 ∨           C	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En 36.0 V +12V 11.78 V ILCC 0.195 A 0.206 A	V +3.3V 3.36 V 3.36 V 3.35 V 3.36 V UM TIME 011 s I +12V 0.769 A Rx1 757 µW 719 µW	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A 0.000 A V +3.3' 3.36 V Rx2 706 µW 665 µW	<ul> <li>V V+3.3V</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>0.396 A</li> <li>0.396 A</li> <li>Rx3</li> <li>706 µW</li> <li>665 µW</li> </ul>	I + 3.33         I + 5.33           V         115.00           V         115.00           V         0.00 r           V         116.00           V         116.00           V         0.00 r           J         5.05 V           Rx4         Sta           722 µW         450           674 µW         450	MA nA mA mA nA 1 +5V 0.349 rt-Up 0 ms 3 ms
lots           Slot           1           2           3           4           unning           Power           Good           34           Time           00:27:           SFP           QSFP           1           2	PCIe L 0-: 0-: 0-: g Status r Pow 29 29 29 29 29 29 29 29 29 29	anes 3 3 7 7 7 8 7 1 ms ate DN	Port 1 2 4 5 Tit 00:0 TPEX 59° C C C C C C C C C C C C C C C C C C C	Card           Yes           Yes           No           me         \$           7:09           T CPU           31° C           TX         R           ON         Go	Link Up Up Up 	Speed         Gen3           Gen3         Gen3           Gen3         -           eset         Re           89         T U9           C         31°           os Counte         0           0         0	Width           x2           x4           x8           -           set         Re           1         T US           2         30°           r         Tem           35° (         37° (	V + 12V           11.78 V           11.78 V           11.78 V           11.78 V           11.78 V           102 ms           D1           T U92           C           29° C           P           Vcc           C           3.32 V           C	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIE En 36.0 V +12V 11.78 V ILCC 0.195 A 0.206 A	V +3.3V 3.36 V 3.36 V 3.35 V 3.35 V 3.36 V UM Time D11 s I +12V 0.769 A Rx1 757 µW 719 µW	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A 0.000 A V +3.3' 3.36 V Rx2 706 µW 665 µW	<ul> <li>V +3.3V</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>0.396 A</li> <li>0.396 A</li> <li>Rx3</li> <li>706 µW</li> <li>665 µW</li> </ul>	/aux         I + 3.33           √         I 15.00           ∨         115.00           ∨         0.00 r           ∨         116.00           ∨         0.00 r           ∨         116.00           ∨         0.00 r           ∨         5.05 ∨           Rx4         Sta           722 µW         45t           674 µW         45t	mA mA mA nA nA <b>I +5V</b> 0.349 <b>rt-Up</b> 0 ms 3 ms
ots Slot 1 1 2 3 3 4 Inning Power Good 34 Time 00:27: 5FP 1 2 Inning FAN FAN	PCIe L 0-: 0-: 0-: g Status r Pow 29 29 29 29 29 29 29 29 29 29	anes 3 3 7 7 rer Up 1 ms ate DN FAN 2 000 02	Port 1 2 4 5 Tit 00:0 TPEX 59° C C C C C C C C C C C C C C C C C C C	Card Yes Yes No TCPU 31° C Tx R ON Go ON Go	Link Up Up Up  Since R 00:07 33° X L od od AN 4	Speed         Gen3           Gen3         Gen3           Gen3         -           eset         Re           :08         T U9           C         31°           os Counte         0           0         0	Width           x2           x4           x8           -           set         Re           1         T US           2         30°           r         Tem           35° (         37° (	V + 12V           11.78 V           11.78 V           11.78 V           11.78 V           11.78 V           102 ms           01           102 ms           02           29° C           P           Vcc           C           3.32 V           C	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIE En 36.0 V +12V 11.78 V ICC 0.195 A 0.206 A	V +3.3V 3.36 V 3.36 V 3.35 V 3.35 V UM Time D11 s I +12V 0.769 A Rx1 757 μW 719 μW	I +3.3V           0.117 A           0.000 A <t< td=""><td><ul> <li>V +3.3V</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>0.396 A</li> <li>0.396 A</li> <li>Rx3</li> <li>706 µW</li> <li>665 µW</li> </ul></td><td>/aux         I + 3.33           √         I 15.00           ∨         115.00           ∨         0.00 r           ∨         116.00           ∨         0.00 r           √         V + 5VSB           ↓         5.05 ∨           Rx4         Sta           722 μW         450           674 μW         450</td><td>mA mA mA mA nA 1+5V 0.349 0 ms 3 ms</td></t<>	<ul> <li>V +3.3V</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>0.396 A</li> <li>0.396 A</li> <li>Rx3</li> <li>706 µW</li> <li>665 µW</li> </ul>	/aux         I + 3.33           √         I 15.00           ∨         115.00           ∨         0.00 r           ∨         116.00           ∨         0.00 r           √         V + 5VSB           ↓         5.05 ∨           Rx4         Sta           722 μW         450           674 μW         450	mA mA mA mA nA 1+5V 0.349 0 ms 3 ms
bits           Slot           1           2           3           4           Dower           Dower           Good           44           Time           00:27:           SEFP           2           1           2           1           2           1           2           SEFP           SEFP           FAN           830 R	PCIe L           0-:           0-:           0-:           0-:           0-:           0-:           0: </td <td>anes 3 3 7 7 5 6 7 7 7 7 7 7 7 7 7 7 7 7 7</td> <td>Port           1           2           4           5           Tir           00:0           T PEX           59° C           ate           0DN           0DN           FA           M</td> <td>Card           Yes           Yes           No           me         1           7:09           T CPU           31° C           TX         R           ON         Go           ON         Go           N         3</td> <td>Link Up Up - 00:07 33° X L od od RPM</td> <td>Speed         Gen3           Gen3         -           Gen3         -           eset         Re           08         T U9           C         31°           os         Counter           0         0</td> <td>Width           x2           x4           x8           -           set         Re           1         T US           2         30°           r         Tem           33° (         37° (</td> <td>V + 12V           11.78 V           11.78 V           11.78 V           11.78 V           11.78 V           102 ms           D1           T U92           C         29° C           P         Vcc           C         3.32 V           C         3.32 V</td> <td>I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIE En 36.0 V +12V 11.78 V ILCC 0.195 A 0.206 A</td> <td>V +3.3V 3.36 V 3.36 V 3.35 V 3.35 V 4.10 V 0.11 s I +12V 0.769 A Rx1 757 μW 719 μW</td> <td>I +3.3V 0.117 A 0.000 A 0.0000 A 0.0</td> <td><ul> <li>V V+3.3\ 3.31         3.31         3.31         3.31         3.31         3.31         3.31         3.31         0.396 μ Rx3         706 μW         665 μW         </li> </ul></td> <td>Vaux         I + 3.33           V         115.00           V         0.00 r           V         116.00           V         116.00           V         116.00           V         0.00 r           X         5.05 V           Rx4         Sta           722 μW         45           674 μW         45</td> <td>mA mA mA mA nA 1+5V 0.349 rt-Up 0 ms 3 ms</td>	anes 3 3 7 7 5 6 7 7 7 7 7 7 7 7 7 7 7 7 7	Port           1           2           4           5           Tir           00:0           T PEX           59° C           ate           0DN           0DN           FA           M	Card           Yes           Yes           No           me         1           7:09           T CPU           31° C           TX         R           ON         Go           ON         Go           N         3	Link Up Up - 00:07 33° X L od od RPM	Speed         Gen3           Gen3         -           Gen3         -           eset         Re           08         T U9           C         31°           os         Counter           0         0	Width           x2           x4           x8           -           set         Re           1         T US           2         30°           r         Tem           33° (         37° (	V + 12V           11.78 V           11.78 V           11.78 V           11.78 V           11.78 V           102 ms           D1           T U92           C         29° C           P         Vcc           C         3.32 V           C         3.32 V	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIE En 36.0 V +12V 11.78 V ILCC 0.195 A 0.206 A	V +3.3V 3.36 V 3.36 V 3.35 V 3.35 V 4.10 V 0.11 s I +12V 0.769 A Rx1 757 μW 719 μW	I +3.3V 0.117 A 0.000 A 0.0000 A 0.0	<ul> <li>V V+3.3\ 3.31         3.31         3.31         3.31         3.31         3.31         3.31         3.31         0.396 μ Rx3         706 μW         665 μW         </li> </ul>	Vaux         I + 3.33           V         115.00           V         0.00 r           V         116.00           V         116.00           V         116.00           V         0.00 r           X         5.05 V           Rx4         Sta           722 μW         45           674 μW         45	mA mA mA mA nA 1+5V 0.349 rt-Up 0 ms 3 ms
ots Slot 1 1 3 3 4 Unning Power Good 34 Time 00:27: SFP 2 SFP 1 2 FAN 1830 R 34 Power 4 2 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 3 3 4 4 3 3 4 4 5 5 5 5 5 5 5 5 5 5 5 5 5	PCIe L 0-: 0-: 0-: 0-: 0-: 0-: 0-: 0-:	anes anes a anes anes	Port         1           2         4           5         Tit           00:0         TPEX           559° C         S59° C           ate         1           0DN         1           FA         0	Card           Yes           Yes           No           me         \$           7:09           T           T           CPU           31° C           TX           R           ON           GO           N           S           TX           R           ON           GO	Link Up Up - Since R 00:07: X L od od AN 4 RPM	Speed         Gen3           Gen3         -           eset         Re           89         T US           C         31°           os Counte         0           0         0	Width           x2           x4           x8           -           set         Re           1         T US           2         30°           r         Tem           35° (         37° (	V + 12V           11.78 V           11.78 V           11.78 V           11.78 V           11.78 V           102 ms           01 T U92           C 29° C           P Vcc           C 3.32 V           C 3.32 V	I +12V 0.010 A 0.196 A 0.437 A 0.437 A 0.437 A 0.437 A 0.437 A 0.437 A 0.437 A 0.437 A 0.195 A 0.206 A	V +3.3V 3.36 V 3.35 V 3.35 V 3.35 V 3.35 V 3.36 V UM Time D11 s I +12V 0.769 A Rx1 757 µW 719 µW	I +3.3V 0.117 A 0.000 A 0.000 A 0.000 A 0.000 A V +3.3' 3.36 V R×2 706 µW 665 µW	<ul> <li>V +3.3V</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>0.396 J</li> <li>0.396 J</li> <li>Rx3</li> <li>706 µW</li> <li>665 µW</li> </ul>	/aux         I + 3.33           √         115.00           ∨         115.00           ∨         0.00 r           ∨         116.00           ∨         116.00           ∨         116.00           ∨         0.00 r           ×         116.00           ∨         0.00 r           ×         5.05 ∨           Rx4         Stat           722 µW         45:           674 µW         45:	mA mA mA mA nA 0.349 rt-Up 0 ms 3 ms
ots           Slot           1           2           3           4           unning           Power           Good           34           Time           00:27:           SFP           QSFP           1           2           Ins           FAN           1830 R           3.3VS3           3.3VS3	PCIe L           0-:           0-:           0-:           0-:           0-:           0-:           0:	anes anes anes anes anes anes anes anes	Port           1           2           4           5           Tir           00:0           TPEX           59° C           ate           DN           FA           M           01           3.33	Card           Yes           Yes           Yes           Yes           Tropu           31° C           Tx           R           ON           GO           N           J           Tx           R           QON           GO           ON           GO           Yes           Yes	Link Up Up - since R 00:07: 33° x L ad ad ad ad ad ad ad ad ad ad ad ad ad	Speed         Gen3           Gen3         Gen4           Gen3         -           eset         Re           08         T U9           C         31°           OS Counte         0           0         0	Width           x2           x4           x8           -           set         Re           1         T US           30°           33° (           37° (	V + 12V           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           11.78 ∨           102 ms           01 T U92           C 29° C           9 Vcc           C 3.32 ∨           2 3.32 ∨           QSFP2 3.3	I +12V 0.010 A 0.196 A 0.437 A 0.000 A PCIe En 36.0 V +12V 11.78 V ICC 0.195 A 0.206 A V PEX	V +3.3V 3.36 V 3.35 V 3.35 V 3.35 V 3.35 V 1 +12V 0.769 A Kx1 757 µW 719 µW 2 V 4 V 719 µW	I +3.3V           0.117 A           0.000 A	<ul> <li>V +3.3V</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>3.31</li> <li>0.396 A</li> <li>Rx3</li> <li>706 µW</li> <li>665 µW</li> </ul>	/aux         I + 3.33           √         115.00           ∨         115.00           ∨         0.00 r           ∨         116.00           ∨         116.00           ∨         0.00 r           √         116.00           ∨         0.00 r           ×         5.05 ∨           Rx4         Sta           722 µW         45:           674 µW         45:	mA mA mA mA mA nA 0.349 0.349 0 ms 3 ms

## 10.4.2 Status Page

#### 10.4.2.1 Configuration

#### Table 10-12. Board Information.

Field	Description
HW REV	The board assembly revision
FW REV	The board firmware revision

Field	Description
Serial Number	The serial number of the board used in the PCIe switch configuration space
	and as the MAC address
PCIe Switch	PEX8734 – PCle switch part number

#### Table 10-13. DIP Switch.

Field	Description
S1-S8	The DIP switch status

## Table 10-14. QSFP Configuration.

Field	Description
QSFP	The QSFP number on the board
Present	The presence status
Port	The PCIe switch port number connected to the QSFP
PCIe Lanes	The PCIe lane numbers connected to the QSFP
Vendor	The QSFP vendor name
Part Number	The QSFP part number
Serial Number	The QSFP serial number
Technology	The QSFP technology as defined in the QSFP specification.

## Table 10-15. Cable Interface Configuration.

Field	Description
Port	The PCIe switch port number connected to the QSFP
Max Speed	The maximum speed supported by the cable port
Max Width	The maximum width supported by the cable port. The width depends on
	the number of installed QSFPs.

### Table 10-16. Slot Configuration.

Field	Description
Slot	The slot number
PCle Lanes	The PCIe connector lanes assigned to the port
Port	The PCIe switch port number assigned to the PCIe lanes
Max Speed	The maximum speed supported by the slot
Max Width	The maximum width supported by the slot

## 10.4.2.2 Status

## Table 10-17. Cable Interface Status.

Field	Description
Port	The PCIe switch port number connected to the QSFP
Link	The link status
Speed	The negotiated speed
Width	The negotiated width
Recovery	The recovery state counter. The counter is used to evaluate the link quality.
	It should not change during the operation. A slow increment is acceptable.
Rx Error	The receiver error counter. The counter is used to evaluate the link quality. It
	should not change during the operation. A slow increment is acceptable.

Field	Description
Bad TLP	The bad TLP counter. The counter is used to evaluate the link quality. It
	should not change during the operation. A slow increment is acceptable.
Bad DLL	The bad DLL counter. The counter is used to evaluate the link quality. It
	should not change during the operation. A slow increment is acceptable.
Width Retrain	The number of times the H18 tried to retrain the link to the maximum
	width. The link must train before the PCIe enumeration starts.

## Table 10-18. Slots Status.

Field	Description
Slot	The slot number
PCIe Lanes	The PCIe connector lanes assigned to the port
Port	The PCIe switch port number assigned to the PCIe lanes
Card	The card presence status
Port	The PCIe switch port number connected to the PCIe slot
Link	The link status
Speed	The negotiated speed
Width	The negotiated width
V +12V	The +12V slot voltage
I +12V	The +12V slot current
V +3.3V	The +3.3V slot voltage
I +3.3V	The ++3.3V slot current
V +3.3Vaux	The +3.3Vaux slot voltage
I +3.3Vaux	The +3.3Vaux slot current

## Table 10-19. Running Status.

Field	Description
Power	The power supply status
Power Up	The time required to turn on the main power supply
Time	The time from the R34 power-up
Since Reset	The time since the last reset
Reset	The number of resets from the computer power-up
Reset Length	The length of the last reset pulse
PCIe Enum Time	The time from the last reset to the start of the PCIe switch enumeration.
	This time must be longer than the time required to turn on the remote
	device.

### Table 10-20. R34 Status.

Field	Description
Time	The elapsed time from powering the R34 by the main power supply standby
	voltage
State	The R34 state
T PEX	The PCIe switch junction temperature. The maximum operating junction
	temperature is 110 <sup>o</sup> C.
T CPU	The junction temperature of the supervisory CPU. Maximum Tj = $125^{\circ}$ C
T U89	The U89 temperature
T U90	The U90 temperature

Field	Description
T U91	The U91 temperature
T U92	The U92 temperature
V +12V	The +12V main power supply voltage
I +12V	The +12V main power supply current
V +3.3V	The +3.3V main power supply voltage
I +3.3V	The +3.3V main power supply current
V +5VSB	The +5VSB main power supply voltage
I +5VSB	The +5VSB main power supply current

## Table 10-21. QSFP Status.

Field	Description
QSFP	The QSFP number on the board
Power	The power supply powering the QSFP
State	The QSFP state
Тх	The transmitter status
Rx	The receiver status
LoS Counter	The Loss of Signal counter from the last reset
Temp	The internal QSFP temperature
Vcc	The internal QSFP voltage
lcc	The QSFP current
Rx1-Rx4	The measured Rx power
Start-Up	The QSFP initialization time
I2C Error	The number of I2C errors since the last reset

## Table 10-22. Fans Status.

Field	Description
FAN 1	The FAN 1 status and RPM
FAN 2	The FAN 2 status and RPM
FAN 3	The FAN 3 status and RPM
FAN 4	The FAN 4 status and RPM

## Table 10-23. R34 Internal Power Supplies.

Field	Description
3.3VSB	The 3.3V standby power supply voltage
CPU 1.8V	The CPU 1.8V power supply voltage
3.3Vaux	The 3.3Vaux power supply voltage
QSFP 3.3V	The QSFP 3.3V power supply voltage
QSFP1 3.3V	The QSFP 1 3.3V power supply voltage measured on the connector
QSFP2 3.3V	The QSFP 2 3.3V power supply voltage measured on the connector
PEX 1.8V	The PCIe switch 1.8V power supply voltage
PEX 0.9V	The PCIe switch digital 0.9V power supply voltage
PEX 0.9VA	The PCIe switch analog 0.9V power supply voltage

#### **10.4.3 Backplane Configuration Page**

#### *Figure 5. R34 Backplane Configuration Page*

		Adnacom R34		
Status	<b>Backplane Configuration</b>	Network Configuration	Firmware Update	Help
Slot Config	uration			
<ul> <li>Slots are configured by DIP switches S1.1 and S1.2</li> <li>Slots are configured by settings on this page</li> </ul>				
Slot 1: 1 Port	x4 ~			

Slot 3:	1 Port x8	~

Slot 4: 1 Port x8 ~

Slot 2: 1 Port x4

#### Fan Configuration

Fan	Sensor	Profile	T1 ℃	PWM1	T2 °C	PWM2	<b>T3</b> ℃	PWM4	<b>T4</b> ℃	PWM4	T5 °C	PWM5
1	PEX ~	Silent ~	20	20	35	30	50	40	65	50	80	100
2	PEX ~	Silent ~	20	20	35	30	50	40	65	50	80	100
3	PEX ~	Silent ~	20	20	35	30	50	40	65	50	80	100
4	PEX ~	Silent ~	20	20	35	30	50	40	65	50	80	100

Save Configuration

#### Fan Test

Fan	Test Enable	Control	PWM	RPM
1		Off ~		- 0
2		Off ~		- 0
3		Off ~		- 0
4		Off ~		- 0

#### **10.4.3.1 Slot Configuration.**

- 1. Select the required slot configuration control using two radio buttons.
- 2. Select the required slot configuration using the DIP switches or drop-down lists.
- 3. Save the selected configuration by clicking on the Save Configuration button.

#### **10.4.3.2 Fan Configuration**

#### Table 10-24. Fan Speed Temperature Sensors.

Field	Description
PEX	The fan speed is controlled by the PCIe switch temperature sensor (PEX)
Board	The fan speed is controlled by the board temperature sensor (CPU)
QSFP	The fan speed is controlled by the optical QSFP temperature sensor (QSFP). If the QSFP sensor is not available, the fan speed is controlled by the board
Disabled	The fan is disabled

## Table 10-25. Fan Profile.

Field	Description
Silent	The predefined profile
Normal	The predefined profile
Custom	The user-defined profile

The profile consists of five temperature and PWM pairs. The fan is OFF if the sensor temperature is below the T1. If the sensor temperature is above the T5, the fan PWM is equal to the PWM5.

After the fans are configured, save the configuration by clicking on the Save Configuration button.

#### 10.4.3.3 Fan Test

For testing and evaluation purposes, the controls in the Fan Test section allow testing the PWM settings, measuring the RPM, and evaluating the fan performance when the R34 is ON.

## **11 Troubleshooting**

### 11.1 Overview

The goal of troubleshooting is to find and fix a problem that prevents the system from operating as the application requires. The recommended troubleshooting principles are as follows:

- 1. Identify the problem: What exactly is not working?
- 2. Establish a theory of probable cause: What part of the system may cause such failure, or what has changed since the last time the system operated properly?
- 3. Test the theory: Replace the component which may cause the problem or change its state. Change only one thing at a time.
- 4. Verify the system functionality. If the problem is fixed, continue to step 5. Otherwise, revert changes made in step 3 and return to step 2.
- 5. Document the findings, actions, and outcomes.

### **11.2 System Context Diagram**

The PCIe extension consists of the following components: a computer, an H18 host adapter, a QSFP cable, an R34 backplane, an R34 power supply, and add-in cards installed in the R34 slots. The components are connected via interfaces shown in Figure 11-1. The diagram shows the components and interfaces that should be analyzed, changed, and tested during troubleshooting.



### Figure 11-1. S31 System Context Diagram.

## **11.3 Troubleshooting Algorithm**

#### **11.3.1 Identify Problem**

Describe the problem in detail and analyze the system components and interfaces to identify the most probable component or interface which can cause the problem. If the problem is real and most likely caused by the S31 system, continue to the next section. Otherwise, please consult the documentation of other components and request technical support from their manufacturers.

### **11.3.2 Review Operating and Installation Instructions**

The operation and installation instructions are provided in sections 4 and 5, respectively. If the system is installed correctly, it is recommended to remove the H18 from the computer and install it step-by-step, as described in the following sections.

### 11.3.3 Verify Computer and Add-in Card

After the H18 is removed from the computer, install the add-in card into the computer and verify that the computer and add-in card operate correctly.

#### 11.3.4 Verify H18 Host Adapter

Install the H18 into the computer without the QSFP cable. Verify that the red standby LED is ON when the computer is OFF. If the standby LED is OFF, that indicates that there is no +3.3Vaux voltage on the PCIe slot. Check the BIOS settings to enable the voltage or reset the BIOS settings to default values. In DELL computers, +3.3Vaux is enabled by setting BIOS Settings->Power Management-> Deep Sleep Control->Disabled.

Turn on the computer and verify that the H18 is visible by the computer software, as described in section 6. If the H18 is not visible, use the H18 status LEDs and web interface to identify the problem. The H18 LEDs are described in section 7. The web interface described in section 10 provides detailed information about the H18 status and PCIe slot voltages.

If the H18 does not operate correctly, try to install the H18 using a different slot or into a different computer. If it looks like an H18 failure, then continue to section 13.

If no problem with the H18 is identified, then turn off the computer and continue to the next section.

#### 11.3.5 Verify QSFP Cable

Attach the cable to the H18 QSFP connector. Turn on the computer and verify that the H18 is visible by the computer software.

Use the web interface to verify that the H18 detects the cable and that the H18 correctly displays the cable parameters. The H18 reads the cable configuration and status via an I2C interface. There should be no I2C errors detected, and the QSFP state should be ON.

If a problem with the cable is identified, then try a different cable or transceiver. The list of recommended cables is provided in sections 3.2.1 and 3.2.3.

If no problem with the cable is identified, then turn off the computer and continue to the next section.

#### 11.3.6 Verify R34 Backplane

Attach the cable to the R34 QSFP connector. Turn on the R34 using the power switch button on the board. Use the web interface to verify that the R34 detects the cable and that the R34 correctly displays the cable parameters. There should be no I2C errors detected, and the QSFP state should be ON. The cable interface status table displays PCIe link error counters. These counters should not change during operation. If the counters change slowly (once in a few seconds), it does not affect performance but may indicate that the cable quality is marginal.

If a problem with the cable is identified, then try a different cable or transceiver. Verify the main power supply and internal power supply voltages. Turn on the computer and verify that the computer boots and the R34 are visible by the computer software, as described in section 6.

If the R34 is not visible, verify that either the standby or power-on LED is ON. The R34 LEDs are described in section 7.

Use the web interface described in section 10 to identify a possible problem with the R34. If it looks like an R34 failure, then continue to section 13.

If no problem with the R34 is identified, turn off the computer and the R34 and continue to the next section.

### 11.3.7 Verify Add-in Card

Install the add-in card in one of the slots. Verify that the slot is enabled. The slot configuration is set by the DIP switch described in section 8 and on the configuration page described in section 10.4.3. The type of slot configuration is indicated by the D15 LED status when the R34 is turned ON. The S2 and S4 slots can be disabled in some configurations. Turn on the R34 and verify using the web interface that the card is detected and +12V, 3.3V, and 3.3Vaux are applied to the slot. Turn on the computer and verify that the computer boots, the add-in card is visible by the computer software, and there is no problem with the card driver. If the card driver is not installed correctly, reinstall the driver and reboot the computer.

#### **11.4 Operating and Performance Problems**

Use the web interface to identify problems with the PCIe link, cable, power, and environment. The link error counters indicate a problem with the cable or transceivers. The reset and link-down counters may indicate a problem with the power supply.

#### 11.5 Cable Problems

Use the web interface to identify problems with the QSFP transceivers and cables. The receiver's optical power should be above the minimum sensitivity threshold specified in the datasheets. If the threshold is not specified, then the power level should not be less than -11dbm (79  $\mu$ W). The internal voltage and temperature should be within the limits specified in the datasheet.

#### 11.6 R34 Automatic Power ON/OFF Problems

The R34 must be ON and configured when the computer software starts the PCIe bus enumeration; otherwise, it will not be visible by the computer software. The web interface provides measured timing information, which can help to identify the problem. The maximum turn-on time for a standard ATX power supply is 500 ms. The computer firmware wait time before initiating the boot sequence may be set in the BIOS if required.

## **12 Products Design Disclaimer**

The Adnacom products are designed according to PCI Express specifications listed in their respective datasheets. Hence, they should work with all add-in cards and drivers compliant with those PCI Express specifications. Adnacom can only provide limited support with third-party add-in card installations. Please go to <u>13 Customer Support</u> to contact our support team.

## **13 Customer Support**

For the latest Customer Support information, please visit our website at <u>https://adnacom.com/</u>. When contacting us, please make sure to include all the information below and describe your problem in detail to help us understand your problem better.

- 1) Full name
- 2) Company name
- 3) Phone number
- 4) Email address
- 5) Product model number
- 6) Product serial number

- 7) Computer make/model
- 8) OS and version
- 9) Make/model of PCIe cards installed
- 10) LEDs' statuses on all boards
- 11) A detailed description of the problem
- 12) Screenshots of web status pages

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## **14 Warranty**

All of the Adnacom system components are warranted against defects in materials and workmanship for one year from the date of shipment. Adnacom repairs or replaces (at its option), at no charge, any item(s) found to be defective during the warranty period. This warranty includes parts and labor. Proof of purchase is required for any warranty work. The warranty provided herein does not cover defects caused by the owner's failure to follow the User's Guide; the owner's modification of the product; the owner's abuse, misuse, or negligent acts; or power failure or surges, fire, flood, accident, actions of third parties, or other events outside reasonable control. To return defective items, an RMA number must be obtained from Adnacom and marked on the outside of the package before any item(s) is(are) accepted for warranty work. The returned item(s) must be packaged in a manner similar to the manner that it (they) was(were) received. Failure to do so will void the warranty. After obtaining the RMA number and properly packaging the defective item(s), please ship the package to the address indicated on our website <u>https://adnacom.com/</u>. Please make sure the package label indicates the RMA number provided.

Except as specified above, Adnacom makes no warranties, express or implied, and specifically disclaims any warranty of merchantability or fitness for a particular purpose. Customers' right to recover damages caused by fault or negligence on the part of Adnacom is limited to the amount paid by the customer. Adnacom is not liable for damages resulting from loss of data, profits, use of products, or incidental or consequential damages, even if advised of the possibility thereof.