Adnaco Technology Inc.

System connectivity beyond imagination

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Adnaco-RA Remote Chassis

PCI Express over fiber optic

Small form factor modules

Contents

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Acronyms

RA Acronym	Description
CON	Adnaco-RA connector with PCIe Host functionality.

Acronym	Description
Adnaco-BUS	PHY and logical protocol above PCI-SIG PCI Express specifications, which is compatible with PCI Express Gen1 and Gen2
SFP	Small Formfactor Pluggable Transceiver
Adnaco-H1A	Adnaco Host controller, which is support communication up to 5 Gb/s and compatible with PCIe Gen1 and Gen2
Adnaco-RA3	2x PCIe slots and 2x PCI slots expansion chassis over fiber optic
Adnaco-RA5	RA3 + 2x USB 3.0 ports based on TI Ind. Temp. Range TUSB7320 or TUSB7340
Adnaco-RA5B	RA3 + 2x USB 3.0 ports based on Renesas Ind. Temp. Range UPD720201K8-711-BAC-A
Adnaco-RT1	Chassis reference design for RA3/RA5, schematic available
LaneX	X-number from 0 to 3. Group of signals described PCIe transmit and receive signals. A-TpX, A-TnX, A-RpX, A-RnX.

1 Adnaco-RAx Family Overview

Adnaco-RA3 is a first device from a new small form factor family (Adnaco-RAx) of PCIe over fiber optic extension/expansion. Adnaco-RA3 accepts Adnaco PCIe over fiber optic protocol and converts it to a standard PCI Express bus.
The new Adnaco-RA5 = R1USB30B + RA3 it is combined version of two products slightly more expensive then RA3 and compatible with RA3.

Figure 1 Adnaco-RA3/5 usage diagram

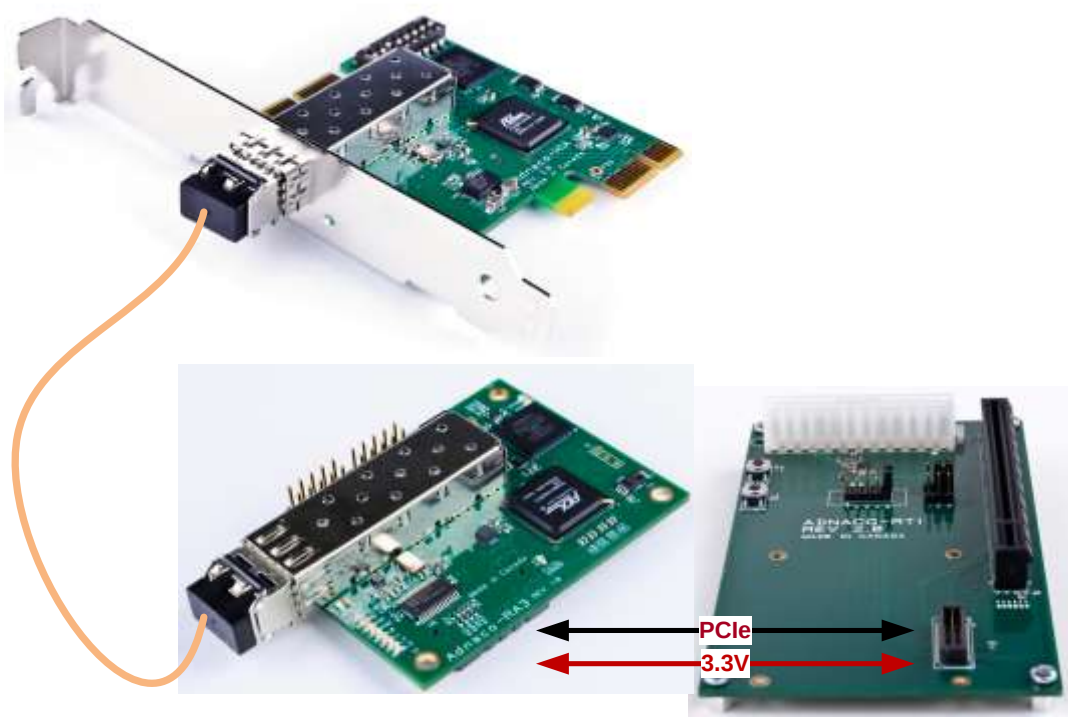


Figure 2 Adnaco-RA5 (preliminary)

TBD picture

2 Technical characteristics

Table 2-1 Adnaco-RAx technical characteristics

	Parameter	Value	Comments
	PCIe support	Up to 5.0 Gb/s	The actual link speed auto-negotiated and depends on customer's board capabilities and support PCIe Gen1 and Gen2
	Distance	from 1 m to several km	Depends on transceivers on RAx and H1A/B boards
	SFP Transceiver	MM or SM	
	Operation temperature		
	Adnaco-RA3 board	-40C…+85C	Board by itself
	Adnaco-RA5 board	-40C…+85C	Board by itself
	Assembly with transceiver #1	-20C…+85C	The temperature range depends on SFP transceiver
	Assembly with transceiver #2	-40C…+85C	The temperature range depends on SFP transceiver
	Power supply	3.3V±10%	Required current depends on RAx board type
	Adnaco-RA3	< 1A	
	Adnaco-RA5	TBD	
	Dimensions	**(L x W x H)**	
	Adnaco-RA3		
	Adnaco-RA5		

3 RAx Signal Description and Connector pin assignment

Adnaco-RA designed as a host according to PCI-SIG definition.

Figure 3 Adnaco-RA3 / RA5 and RA5B Pin Assignment

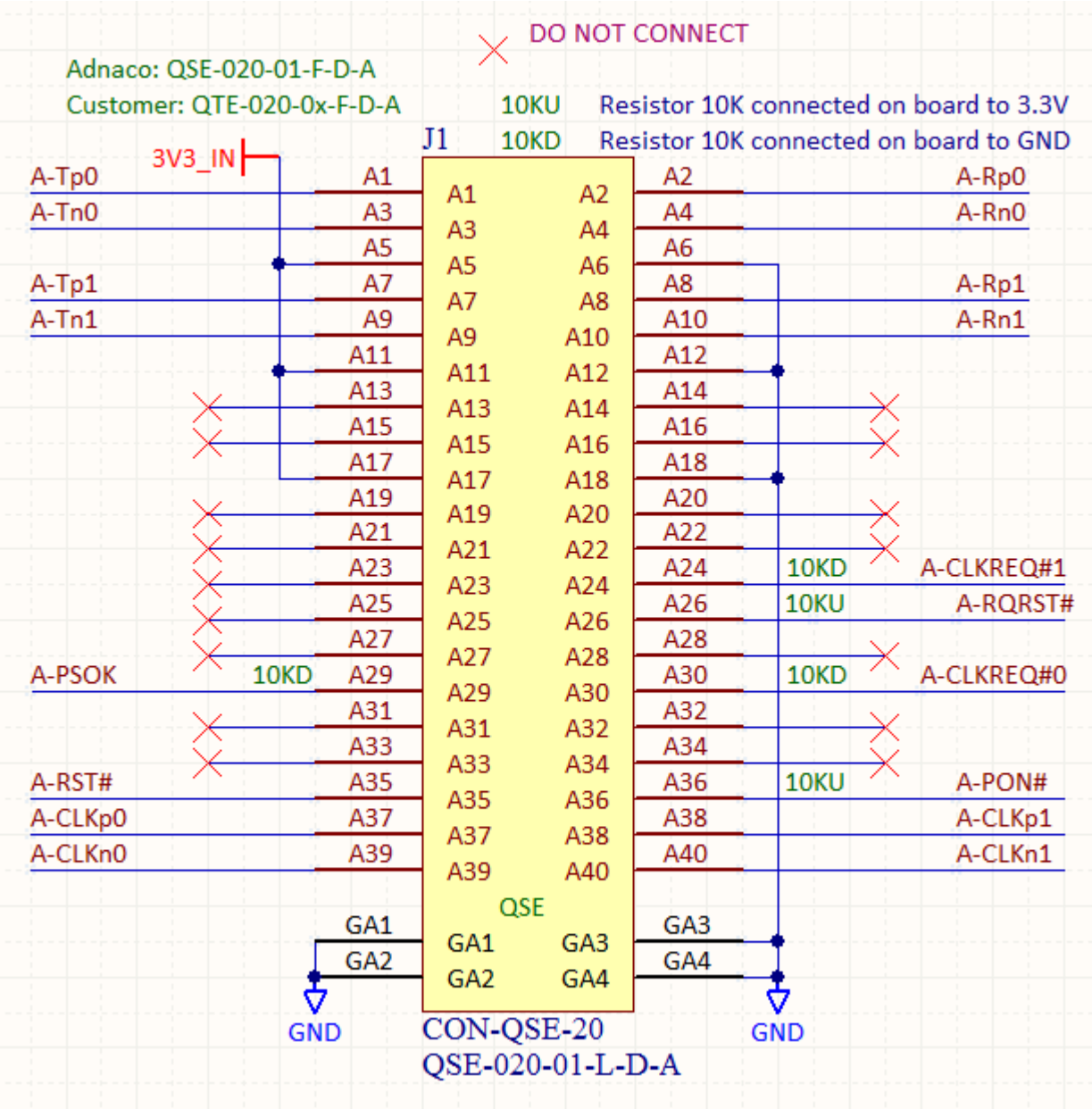


Table 3-1 Signal Description – RAx side

Adnaco signals	PCI-SIG	Description
A-Tp0	PETp0	Output, Transmitter differential pair Lane0
A-Tn0	PETn0	
A-Rp0	PERp0	Input, Receiver differential pair Lane0
A-Rn0	PERn0	
A-Tp1	PETp1	Output, Transmitter differential pair Lane1
A-Tn1	PETn1	
A-Rp1	PERp1	Input, Receiver differential pair Lane1
A-Rn1	PERn1	
A-RST#	PERST#	Output. See PCIe CEM
A-CLKp0	REFCLK+	Output. See PCIe CEM,
A-CLKn0	REFCLK-	
A-CLKn1	REFCLK-	Output. See PCIe CEM
A-CLKp1	REFCLK+	
A-PSOK	ATX spec	Active high. PWR_OK. See ATX power specifications. Has 10K pull down resistor on RAx Boards.
A-PON#	ATX spec	Active low. Has 10K pull up resistor. PS_ON#. See ATX power specifications
A-CLKREQ#X A-CLKREQ#0 A-CLKREQ#1	CLKREQ#	Reference clock request signal. Input. Active low. Has internal 10K resistor connected to GND. Controls state of signal A-CLKp0/1/n0/1. See mini-PCIe specifications. If it is not connected provides active state for A-CLKp0/1/n0/1 signal. Place 1K to 3V3 to have default state for A-CLKp0/1/n0/1 is OFF and have possibility to control A-CLKp0/1/n0/1 signal by A-CLKREQ#X pull down source according to mini-PCIe specifications.
A-RQRST#	-	Active low. Has 10K resistor connected to the 3.3V. Generates a global reset for entire PCIe system propagated from Root Complex to RAx and boards connected to RAx.
3V3	+3.3V	See PCIe CEM
GND	GND	See PCIe CEM

3.1 Adnaco-RAx Signal Support Matrix

Table 2 Adnaco-RAx Features

RA3	RA5 & RA5B	Feature
Gen2 **2x PCIe x1**	**Gen2** **2x PCIe X1**	One Gen2 Upstream Port over fiber optic From two to four Gen2 Downstream ports x1 Compatible with PCIe Gen1
No	**Yes**	Two USB 3.0 Host ports with external +5V power supply for USB ports. Compatible with 2.0.
No	**Yes**	Power supply spread spectrum control

3.2 PCIe and Main Chassis Signals Group

Below a minimum set of signals required to work with Adnaco-RAx device:

- Lanes: A-TpX/nX, A-RpX/nX
- REFCLK: A-CLKpX/nX
- Reset: A-RST#
- A-PSOK provided from power monitor or can be pulled up using 1K connected to 3.3V;

  A-CLKREQ# can be left not connected, in this case A-CLKpX/nX will be always active (X=0,1).

3.3 A-CLKREQ#

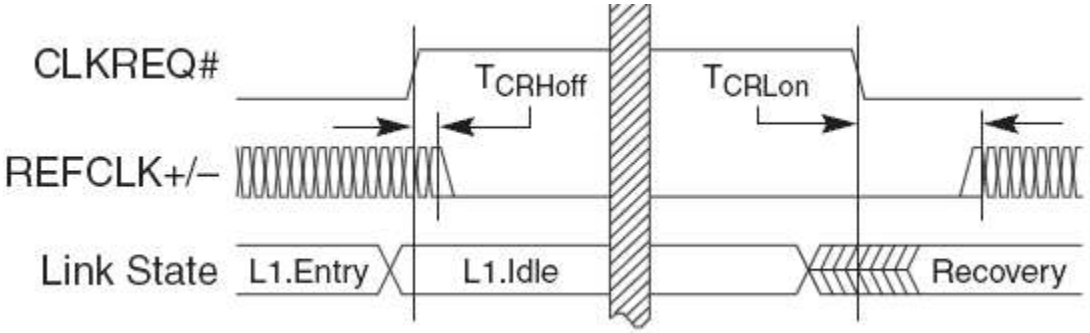
Table 3 Link Capability Register (0x74)

Bit(s)	Description	Ports	Type	Serial EEPROM and I²C	Default
8	**Clock Power Management Enable** ***Reserved*** Read and Writable only when the **Link Capability** register *Clock Power Management Capable* bit is set. The PEX 8604 does ***not support*** removal of the Reference Clock in the L1 and L2/L3 Ready Link PM states.		RsvdP	No	0
11:10	**Active State Power Management (ASPM) Support** Active State Link PM support. Indicates the level of ASPM supported by the Port. 01b = L0s Link PM state entry is supported 11b = L0s and L1 Link PM states are supported All other encodings are ***reserved***.	RO	Yes	11b	
18	**Clock Power Management Capable**	RO	Yes	0	

Adnaco-RA3/4/5 boards reported as no support for clock power management.

PCI-SIG: Support for the CLKREQ# dynamic clock protocol should be reported using bit 18 in the PCI Express link capabilities register (offset 0C4h). To enable dynamic clock management, bit 8 of the Link Control register (offset 010h) is provided. By default, the card shall enable CLKREQ# dynamic clock protocol upon initial power up and in response to any warm reset by the host system. System software may subsequently disable this feature as needed. See PCI Express Base Specification.

Figure 4 CLKREQ# - On/Off control timing (mini-PCIe)



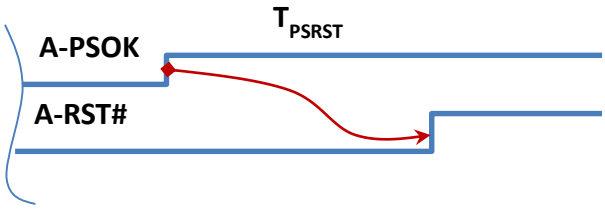
Parameters T_{CRHoff} and T_{CRLon} for A-CLKREQ# < 15 ns.

3.4 System Board Support Signals Group

3.4.1 A-PSOK and A-RST#

A-PSOK is a power good signal and should be asserted high by the power supply to indicate that the +5VDC and +3.3VDC outputs are above the under voltage thresholds of the power supply. When this signal is asserted high, there should be sufficient energy stored by the converter to guarantee continuous power operation within specification. Conversely, when the output voltages fall below the under voltage threshold, or when mains power has been removed for a time sufficiently long so that power supply operation is no longer guaranteed, PWR_OK should be de-asserted to a low state. The recommended electrical and timing characteristics of the PWR_OK signal are provided in the ATX12V Power Supply Design Guide.

Figure 5 A-PSOK and A-RST# diagram



T_{PSRST} equal 1ms ±100 µS.

3.4.2 A-PON#

3.3V in Adnaco-RAx boards behave as +5VSTB except it is 3.3V value.
A-PON# is an active low signal that turns on all of the main power rails including 3.3VDC, 5VDC, -5VDC, 12VDC, and -12VDC power rails. When this signal is held high by the PC board or left open circuited, outputs of the power rails should not deliver current and should be held at a zero potential with respect to ground. Power should be delivered to the rails only if the A-PON# signal is held at ground potential. This signal held at 3V3 by a pull-up resistor.

4 Electromechanical

4.1 RA3 Board Dimensions

Figure 6 RA3 Top View

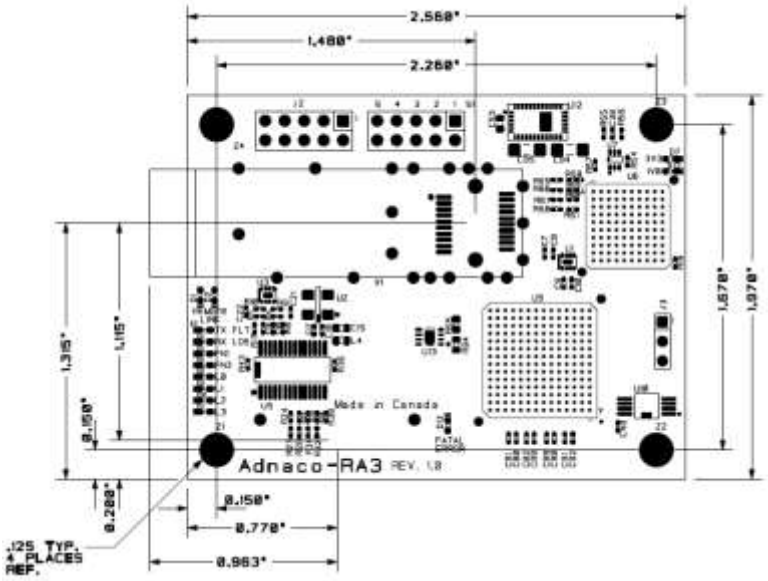
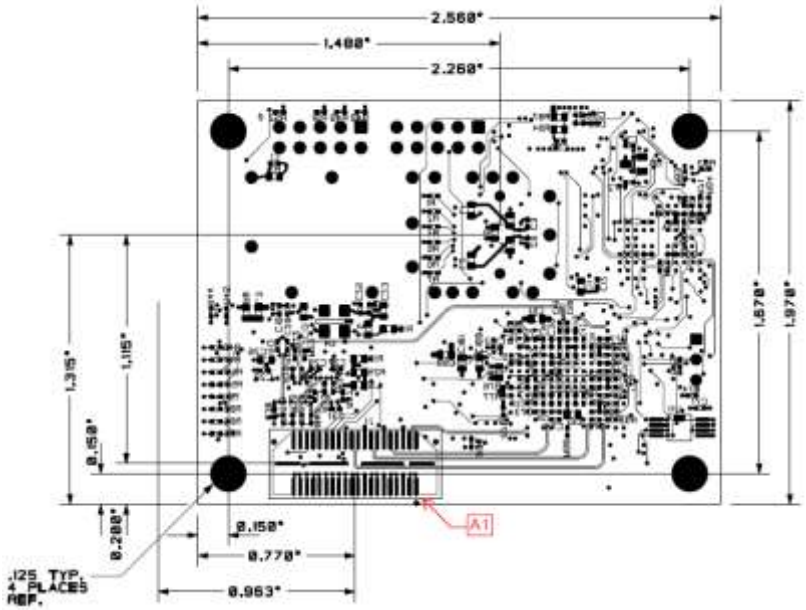
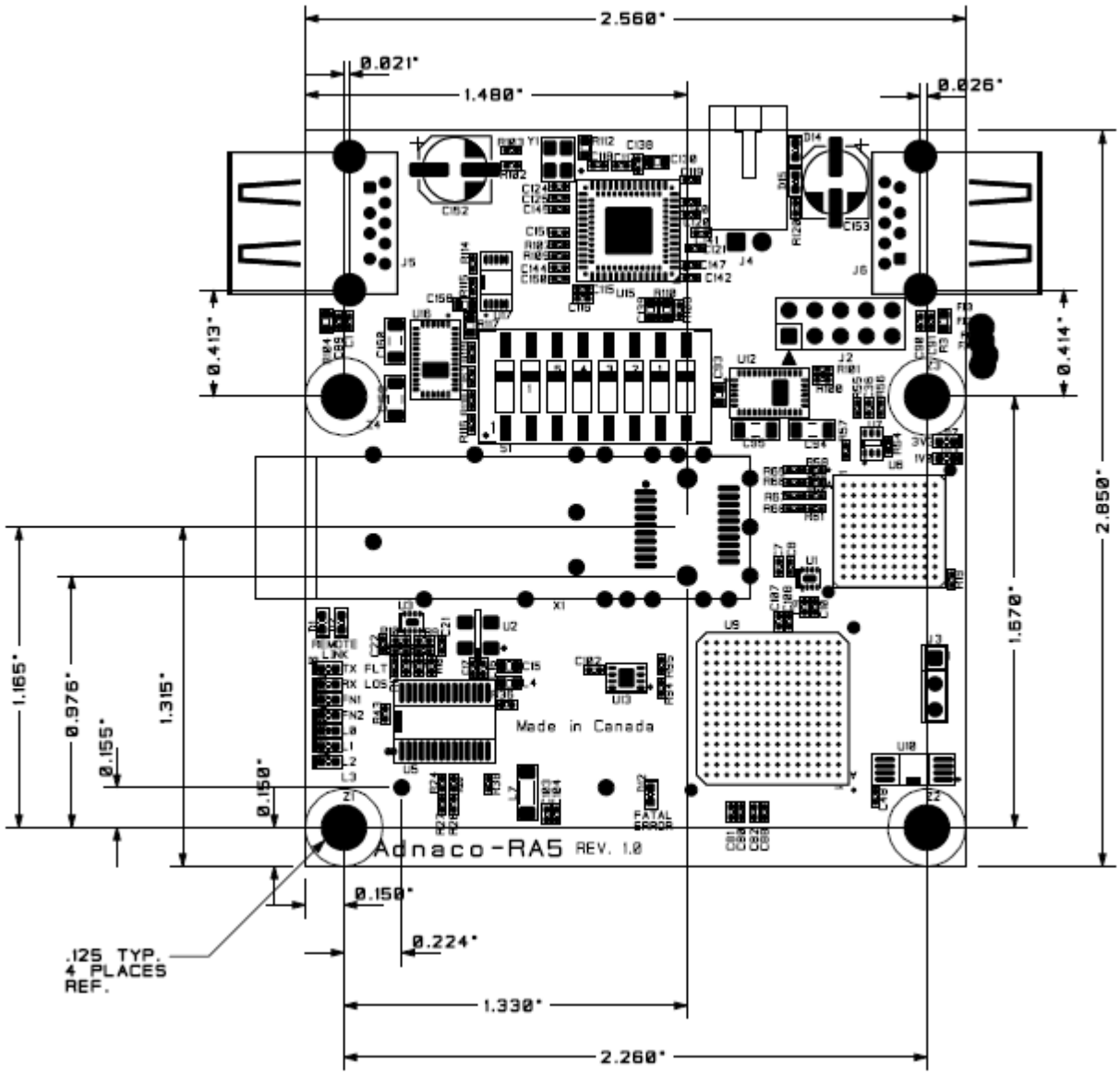


Figure 7 RA3 Bottom View



4.2 RA5 and RA5B Board Dimensions

Figure 8 RA5 Dimensions



4.3 RAx System Connector

Table 4-1 Adnaco-RA3/5 Connectors (Samtec)

Connector Part No	Stack Height	Description
QSE-020-01-F-D-A	NA	Adnaco-RA1/3/4/5 board connector
QTE-020-01-F-D-A	5mm	Customer's connector
QTE-020-02-F-D-A	8mm	Customer's connector
QTE-020-03-F-D-A	11mm	Customer's connector
QTE-020-04-F-D-A QTE-020-04-L-D-A	16mm	Customer's connector

4.4 Recommended Standoff

http://www.samtec.com/ftppub/cpdf/SO-XXXX-XX-XX-XX-X-MKT.pdf

5 PCB layout

Table 2 Adnaco-RA3 Trace Lengths

Signal	Trace Length (1/1000 inch)
A-TN0	907.3
A-TN1	1141.7
A-TP0	904.6
A-TP1	1113.1

Table 3 Adnaco-RT1 Trace Length

Signal	Trace Length (1/1000 inch)
A-PERN0	3988.3
A-PERN1	3989.6
A-PERP0	3989.1
A-PERP1	3990.0
A-PETN0	3989.4
A-PETN1	3990.2
A-PETP0	3989.0
A-PETP1	3989.5

Figure 9 Traces

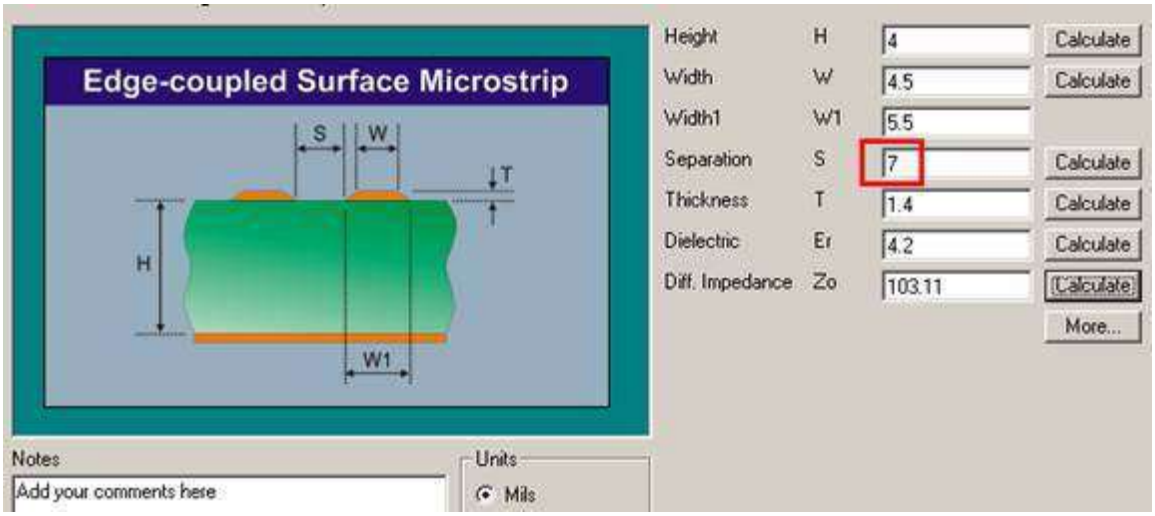


Figure 10 Adnaco-RAx Stackup

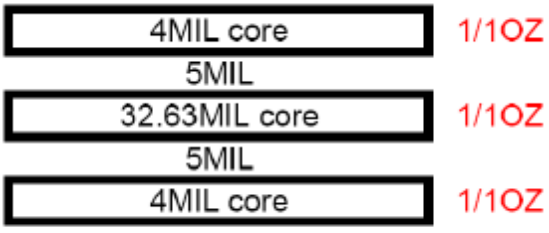
Layer #	Stackup		Thickness (mils)
	solder mask	0.7mil	
	plating		1
L1	signal	1 oz	1.4
	core		4
L2	ground	1 oz	1.4
	prepreg		5
L3	power	1 oz	1.4
	core		32.63
L4	power	1 oz	1.4
	prepreg		5
L5	ground	1 oz	1.4
	core		4
L6	signal	1 oz	1.4
	plating		1
	solder mask	0.7mil	

Total (mils)	**61.03**
Total (mm)	**1.55**

Notes:

1. Outer layers are impedance controlled. Differential impedance is 100 Ohms (+/-15%) for differential pairs with 5 mils width and 5 mils spacing.

2. Thickness between layers L2 and L3 and between layers L4 and L5 should be 4 mils or less



Finish board thickness 1.6mm+/-10%.

Figure 11 Adnaco-RT1 Stackup

Layer #	Stackup		Thickness (mils)	PCB layer
	solder mask	0.7mil		
	plating		1	
L1	signal	1 oz	1.4	CS
	core		4	
L2	ground	1 oz	1.4	CG1
	prepreg		47	
L3	power	1 oz	1.4	CP1
	core		4	
L4	signal	1 oz	1.4	SS
	plating		1	
	solder mask	0.7mil		

Total (mils)	62.6
Total (mm)	1.59

Notes:

1. Outer layers are impedance controlled. Differential impedance is 100 Ohms (+/-15%) for differential pairs with 5 mils width and 7 mils spacing. . Differential impedance is 90 Ohms (+/-15%) for differential pairs with 6 mils width and 7 mils spacing. Differential impedance is 85 Ohms (+/-15%) for differential pairs with 5 mils width and 5 mils spacing.

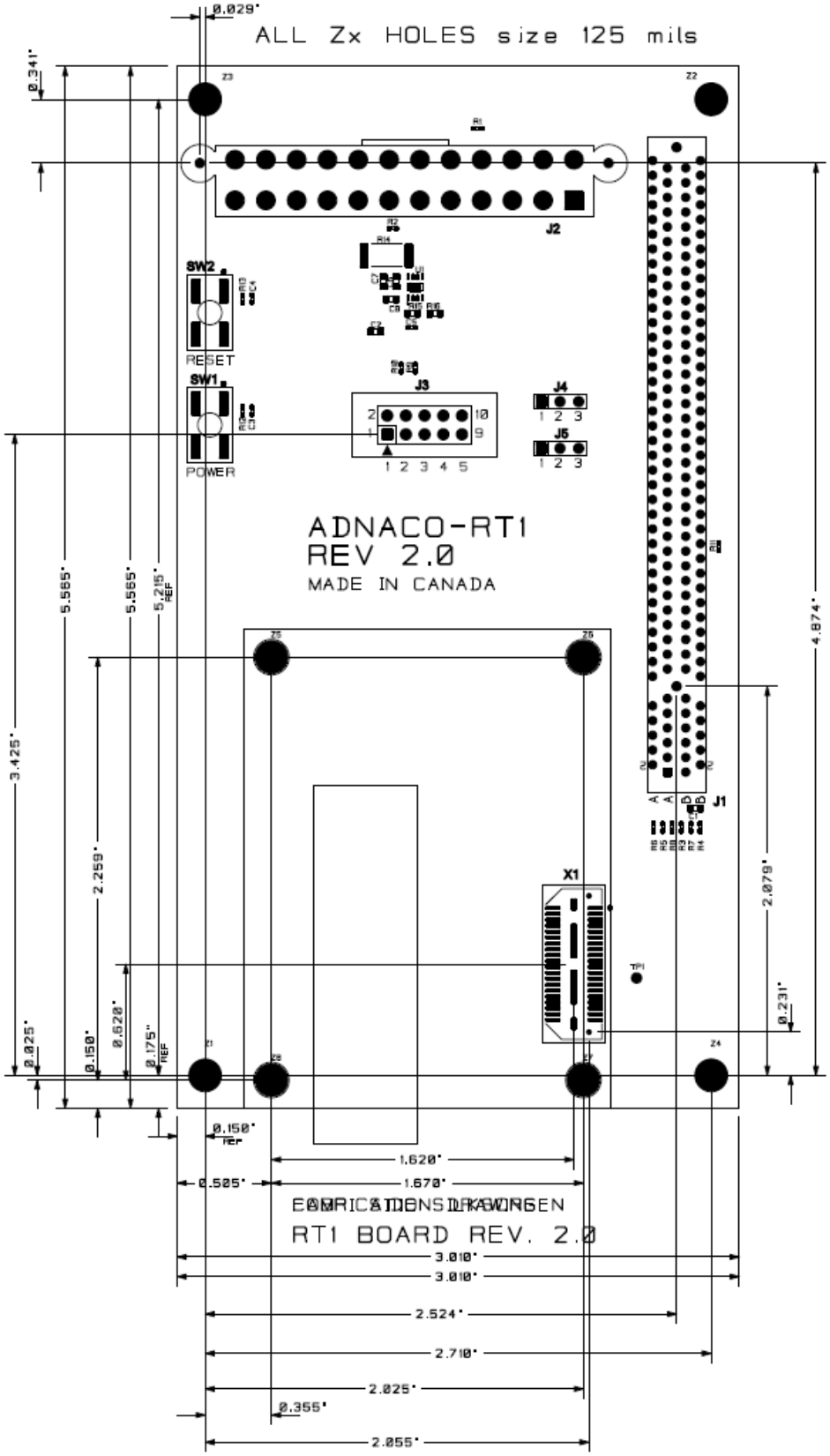
2. Thickness between layers L2 and L3 and between layers L4 and L5 should be 4 mils or less

6 Test Chassis

Figure 12 Adnaco-RT1 Test Board

Figure 13 RA3 + RT1 Assembly

Figure 14 Adnaco-RT1 Dimensions



7 RAx LEDs States and Jumpers and S1 switch Setting

Figure 15 RA3 LEDs Location

Figure 16 RA5 LEDs Location

TBD

Table 4 RA5 S1 Settings

1	2	3	4	5	6	7	8	Description
X								PCIe Ports Configurations
OFF								NO EEPROM
ON								EEPROM0: content TBD
	X							Reserved
		X						PCIe downstream ports reference clock selection
		OFF						100.6 MHz
		ON						101.0 MHz
			X	X	X			Reserved
						X		Power supply clock synchronization (preliminary)
						OFF		No sync
						ON		Synchronized
							X	Power supply spread spectrum control (preliminary)
							OFF	No spread spectrum
							ON	Spread spectrum is ON

Table 5 RA3 Jumper S1 Settings

5	4	3	2	1	Description
			X	X	PCIe Ports Configurations
			OFF	OFF	
			OFF	ON	
			ON	OFF	
			ON	ON	NO EEPROM
		X			PCIe downstream ports reference clock selection
		OFF			100.6 MHz
		ON			101.0 MHz
	X				Reserved
X					Reserved

8 Ordering Information

Table 6 Part Number Builder

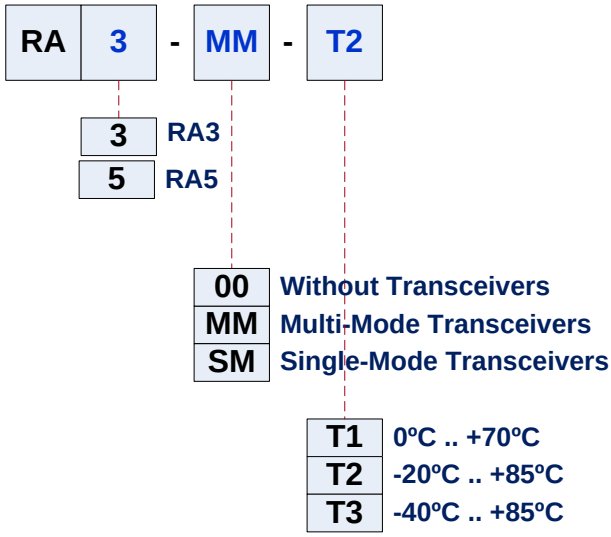


Table 7 Valid Part Numbers List

Valid Part Numbers	Description
RA3-00-T3	
RA3-MM-T2	
RA3-SM-T3	
RA5-00-T3	
RA5-MM-T2	
RA5-SM-T3	

The schematic for the Adnaco-RT1 as a reference design is available upon request.

Figure 17 Adnaco-RT1 Schematic